The Dependence of Material Removal Rate on Annealing Treatment in Polysilicon CMP

Sungmin Park, Haedo Jeong, and Sang-Hee Yoon

***Abstract*—Chemical mechanical polishing (CMP) of polysilicon (poly-Si) films is an essential process in fabricating integrated circuit (IC) devices for high-performance dynamic random access memory (DRAM) and microelectromechanical systems (MEMS) with multi-level structures. Poly-Si films can have changes in surface roughness and grain boundary density (or Young's modulus) through thermal annealing treatment, which exerts a strong influence on poly-Si polishing performance (i.e., uniformity). Here, poly-Si films, after annealing for half hour at 1,050 ℃ under nitrogen atmosphere, are polished to characterize the effect of annealing treatment on their material removal rate (MRR). The dependence of the surface roughness, grain boundary density, and Young's modulus of poly-Si films on annealing treatment is also intensively discussed. The results from this study will help us to establish optimal conditions for poly-Si CMP process.**

***Index Terms*—Annealing, CMP, material removal rate, polysilicon.**

I. Introduction

Poly-Si is a well-known structural material, usually deposited on Si substrate through low-pressure chemical vapor deposition (LPCVD), for microscale devices (e.g., IC devices, sensors and actuators, etc.) due to its excellent mechanical properties [1]. Recently, the continuously increasing degree of integrated functionality (e.g., mechanical, electrical, optoradiative, biochemical, and thermofluidic functions) in the microscale devices leads to the stacking of two (or more than) poly-Si layers. For example, the Sandia Ultraplanar, Multi-level MEMS Technology 5 (SUMMiT VTM) fabrication technology employs five-level poly-Si surface micromachining process [2] to develop a pop-up micromirror. The multiple stacking of poly-Si layers results in inevitable deteriorations in surface planarity due to repeated micromachining processes. A CMP process has been therefore considered and is still being actively studied as a potential method for planarizing uneven surfaces in the fabrication of multi-level microdevices. This is because a CMP process makes it possible to produce a variety of surface micromachined devices with smaller minimum feature sizes, higher aspect ratios, and lower operating voltages (especially, in electrostatic microactuators). In addition, a CMP process is an essential technology for achieving an increase in device complexity by providing the freedom to stack multiple film layers without the limitations caused by large surface topography [3]. Considering the deposition mechanism of a poly-Si film, the residual stress with in the film is an unavoidable consequence, which makes disastrous problems (i.e., film failure) in poly-Si CMP process. In general, a unannealed poly-Si film has a compressive stress of several hundreds. The residual stress in poly-Si can be controlled by several factors such as deposition parameters, thermal annealing, etc [4]. For example, the compressive stress in poly-Si film can be decreased or eliminated to nearly zero through thermal annealing treatment at a temperature of above the deposition temperature [5].

In this paper, we investigate the effect of thermal annealing treatment on the performance of poly-Si CMP process as a fundamental research for the development of poly-Si-based multi-level microdevices. The MRR of a poly-Si film is quantitatively measured as an index of CMP performance. The changes in the surface roughness and grain boundary density (or Young's modulus) of the poly-Si film through thermal annealing treatment are also characterized because the physical properties of the poly-Si film can be altered during thermal annealing treatment [6]. From the characterization results, the dependence of the MRR in poly-Si CMP on thermal annealing process is fully explained.

II. Materials and Methods

A. Sample Preparation

Poly-Si samples for CMP process were prepared by depositing a 0.1 μm-thick SiO_2 film on a 4-inch Si wafer ((100), single-side polished) through thermal oxidation. Next, a 2 μm-thick poly-Si film was deposited on the samples through LPCVD at 545, 585, and 625 ℃. As a final step, each sample was thermally annealed for half hour at 1,050 ℃ under N_2 atmosphere. Amorphous Si wafer was used as a control group in investigating the effect of thermal annealing treatment on the performance of poly-Si CMP process. Totally, four types of samples (i.e., poly-Si samples deposited at 545, 585, and 625 ℃ and amorphous Si sample) were therefore used in this study. The top view images of 4-inch poly-Si sample wafers that were deposited at different temperatures and then thermally annealed are compared to those of amorphous Si sample wafers, as shown in Fig. 1.

B. Poly-Si CMP

A GNP POLI-500 equipped with an endpoint detection system (G&P Technology) was used to polishing samples, as

Manuscript received April 28, 2015; revised July 15, 2015. This work supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science, ICT & Future Planning (NRF-2014R1A1A1006402).

S. Park and S.-H. Yoon are with the Department of Mechanical Engineering, Inha University, Incheon 402-751, Republic of Korea (e-mail: shyoon@inha.ac.kr)

H. Jeong is with the Department of Precision and Mechanical Engineering, Pusan National University, Busan 609-735, Republic of Korea.

DOI: 10.7763/IJMMM.2016.V4.236

shown in Fig. 2(a). A Rodel IC1400 K-groove pad (Rodel), in-situ conditioned with a segment type diamond disk (Ehwa Diamond Industrial Co.), was used as a CMP pad. A P1000 slurry (Cabot Microelectronics) was used in CMP process. The other conditions for poly-Si CMP process were as follows (see Table I): a down-force of 500 g/cm2, a table speed of 60 rpm, a head speed of 60 rpm, and a slurry flow-rate of 150 ml/min. The polisher decided the endpoint of poly-Si layer using its endpoint detection system that measured a friction force signal associated with the CMP process, thus preventing the over-polishing of the samples. In detail, a piezoelectric force sensor was installed on the back of the polishing head to obtain the friction force signal (Fig. 2(b)); the signal from the piezoelectric force sensor was amplified through a charge amplifier and then transferred to a data acquisition board [7]. The monitored friction force signal was used both to determine the moment of over-polishing during CMP process and to analyze the MRR of polished material (i.e., poly-Si and SiO2).

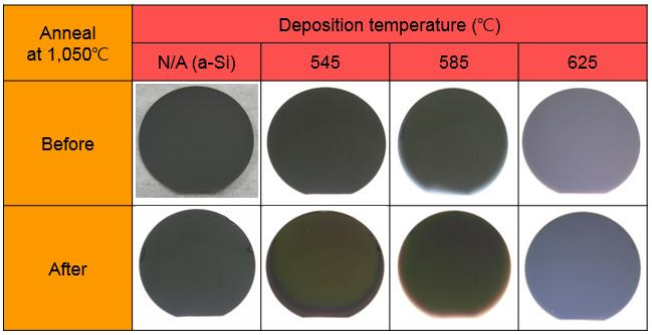

Fig. 1. 4-inch amorphous Si and poly-Si sample wafers as a function of deposition temperature and annealing treatment.

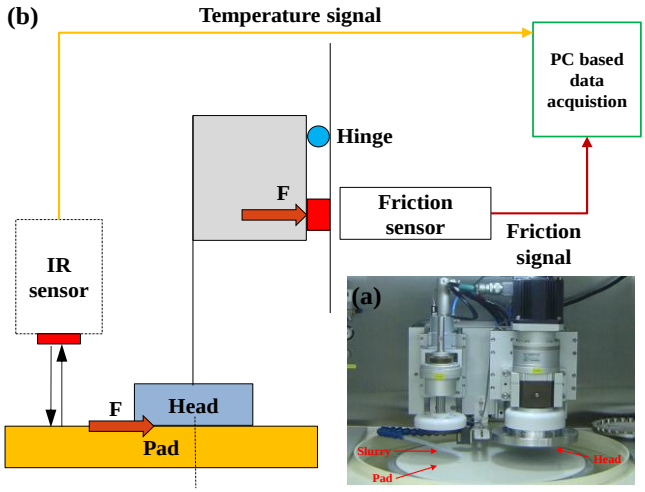

Fig. 2. Experimental apparatus for poly-Si CMP. (a) GNP POLI-500 polisher. (b) Schematic of a CMP system equipped with an endpoint detection system.

C. Physical Properties (Surface Roughness, Grain Boundary Density, and Young's Modulus) Measurement

The change in the surface roughness of the experimental samples through thermal annealing treatment was quantified by measuring their surface profile before and after thermal annealing treatment with a 3D non-contact surface profiler (NV-E1000, Nano System Co., Ltd.). The grain boundary density of the samples was measured with an atomic force microscope (AFM, XE-100, Park Systems Co., Ltd.) before and after thermal annealing treatment. Last but not least, the Young's modulus of each sample was investigated using a customized laser interferometer.

TABLE I: CMP PROCESS CONDITIONS

Parameter	Value
Pressure (down-force)	500 g/cm^2
Table/head speed	60 rpm
Slurry flow-rate	150 cc/min

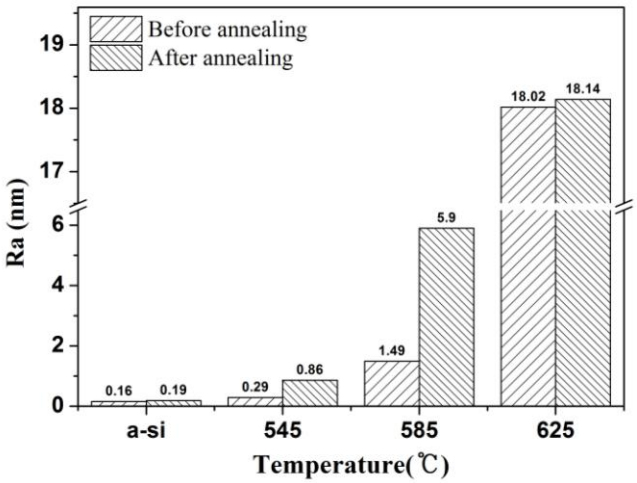

Fig. 3. Variation in the surface roughness of the poly-Si samples before and after thermal annealing treatment as a function of LPCVD temperature, compared with that of the amorphous Si sample.

D. MRR Measurement

The MRR of the polished materials (i.e., poly-Si, amorphous Si) was determined by measuring the thickness of thin films (that is, poly-Si samples deposited at 545, 585, and 625 ℃ and amorphous Si sample (control group)) before and after CMP process. The initial thickness (before CMP) of poly-Si layer was measured by an ellipsometer (AutoEL III, Rudolph Technologies, Inc.). The final thickness (after CMP) was determined by the signals resulted from the endpoint detection system. In detail, based on polishing time and change in film thickness, the MRR of polished materials was calculated. All measurements were made on at least three 4-inch wafers for each sample group (i.e., poly-Si samples deposited at 545, 585, and 625 ℃ and amorphous Si sample). All data were represented as mean values.

III. Results and Discussion

A. Characterization of Physical Properties before and after Thermal Annealing Treatment

The correlation between physical properties and MRR in CMP process are well characterized. Therefore, prior to investigating the dependence of MRR on thermal annealing treatment in poly-Si CMP, the changes in the physical properties (surface roughness, grain boundary density, and Young's modulus) of a poly-Si film through thermal annealing treatment were explored to quantify their effect on the MRR of the poly-Si film.

1) Surface roughness

Among the physical properties of a poly-Si film, the value

of surface roughness (i.e., Ra value) is recognized as one of the most critical factors to determine the polishing rate (i.e., MRR) and uniformity of poly-Si during CMP process [8]. Variation in the surface roughness of the poly-Si samples through thermal annealing treatment is studied as a function of LPCVD temperature, as shown in Fig. 3.

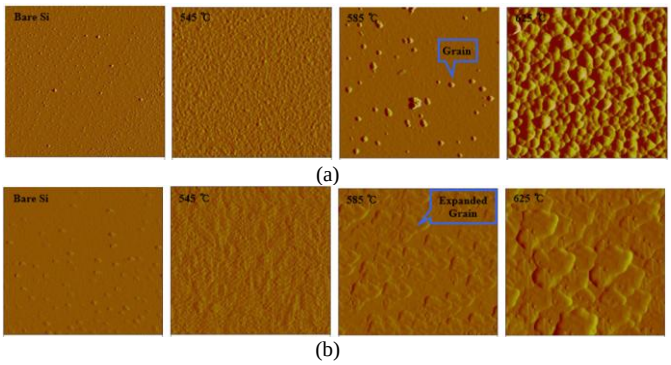

Fig. 4. Change in the surface morphology (i.e., grain boundary density) of the poly-Si samples before (a) and after (b) thermal annealing treatment as a function of LPCVD temperature, compared with that of the amorphous Si sample. The grain boundary density is obtained with AFM.

First of all, as the LPCVD temperature was increased from 545 ℃ to 625 ℃, the surface roughness of the poly-Si sample was increased from 0.29 nm to 18.02 nm. Considering that a high-quality poly-Si film can be deposited at a temperature of about 620 ℃, the increase in surface roughness is unavoidable. Secondly, the surface roughness of the amorphous Si and poly-Si samples was increased within a range of 0.03 to 4.41 nm after thermal annealing treatment at 1,050 ℃ for half hour. The thermal annealing treatment on a poly-Si film had a few drawbacks (i.e., increase in surface roughness), while there were numerous, incomparable benefits resulted from thermal annealing treatment (i.e., residual stress relief, minimization of Ra value difference at a standard LPCVD temperature (that is, 625 ℃), increase in Young's modulus, etc.). This justifies the need for thermal annealing treatment in fabricating multi-level microdevices using poly-Si CMP.

2) Grain boundary density

The surface morphology (especially, grain boundary density) of a poly-Si film which is supposed to be polished with CMP process is also a key factor for determining MRR. This is because grain boundary density is closely related to the Young's modulus of the poly-Si film. Change in the grain boundary density of the poly-Si samples before and after thermal annealing treatment is characterized as a function of LPCVD temperature, as shown in Fig. 4. As the LPCVD temperature was increased, the grain boundary density of the poly-Si film was increased but the grain size was not affected, which is in good agreement with a previous report [4]. The boundaries formed by a set of grains were shown to be extended or combined (see Fig. 4). For the poly-Si film deposited at 625 ℃, the extension of its grain boundaries was apparently measured to be 5.2 times increased through thermal annealing treatment. This indicates that the movement of dislocations in the grains, and reduces a compressive stress [5]. Furthermore, in spite of significant changes in grain boundaries after thermal annealing treatment, the distribution of grain size or boundary was shown to be uniform, thus having no influence on poly-Si MRR during CMP process.

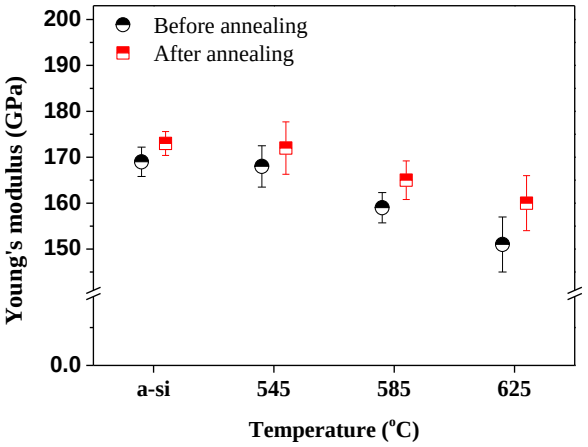

Fig. 5. Change in the Young's modulus of the poly-Si samples through thermal annealing treatment as a function of LPCVD temperature, compared with that of the amorphous Si sample.

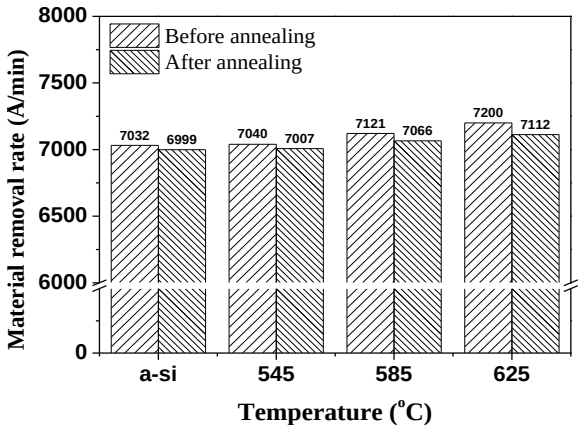

Fig. 6. Change in the MRR of the poly-Si samples through thermal annealing treatment as a function of LPCVD temperature, compared with that of the amorphous Si sample.

3) Young's modulus

The hardness of an elastic material polished by CMP process is firmly linked to the MRR of the material. Young's modulus is a representative measure of material hardness. Thus, a change in the Young's modulus of poly-Si samples through thermal annealing treatment was investigated as a function of LPCVD temperature, as shown in Fig. 5.

The Young's modulus of poly-Si samples was decreased as the LPCVD temperature was increased. Before thermal annealing treatment, the Young's moduli of amorphous Si and three types of poly-Si (545, 585, 625 ℃) were 169±3.2, 168±4.5, 159±3.3, and 151±6.0 GPa, respectively. The Young's modulus was, however, improved through thermal annealing treatment. After thermal annealing treatment, the Young's moduli of amorphous Si and three types of poly-Si (545, 585, 625 ℃) were 173±2.6, 172±5.7, 165±4.2, and 160 ±5.4 GPa, respectively. Young's modulus of a poly-Si film is highly dependent on a change in the number of Si-Si bonds per volume. Thermal annealing treatment leads to the rearrangement of atoms in a poly-Si film. The vacancies in the grains and grain boundaries can be filled and the mass

density increases. Thus, the density of Si-Si bonds per volume and therefore Young's modulus increases.

B. MRR in Poly-Si Cmp

To investigate the effect of thermal annealing treatment on MRR in poly-Si CMP, the MRR of the poly-Si samples before and after thermal annealing treatment is characterized as a function of LPCVD temperature, as shown in Fig. 6. Before thermal annealing treatment, the MRRs of amorphous Si and three types of poly-Si (545, 585, 625 ℃) were 7,032, 7,040, 7,121, and 7,200 Å, respectively. After thermal annealing treatment, the MRRs of amorphous Si and three types of poly-Si (545, 585, 625 ℃) were 6,999, 7,007, 7,066, and 7,112 Å, respectively.

From the experiments, the MRR was inversely proportional to LPCVD temperature and was decreased through thermal annealing treatment. The trends of MRR were exactly matched with those of Young's modulus, explained before. In other words, the decrease in MRR after thermal annealing treatment is due to the increase in poly-Si hardness imposed during thermal annealing treatment. The results indicate that thermal annealing treatment on LPCVDed poly-Si films has slight loss in MRR but significant improvement in their mechanical properties (i.e., residual stress relief). Moreover, we can find the optimal conditions for poly-Si CMP process in fabricating multi-level microdevices on the basis of the experimental results obtained from this study.

IV. Conclusions

We have investigated the effect of thermal annealing treatment on the performance of poly-Si CMP process as a fundamental research for the development of poly-Si-based multi-level microdevices. Thermal annealing treatment on LPCVDed poly-Si films resulted in significant improvement in their mechanical properties which is essential in developing poly-Si-based multi-level microdevices, together with several negative issues including increase in surface roughness and decrease in MRR. The results from this study will help us to form the backbone for establishing optimal poly-Si CMP process conditions. This poly-Si CMP is expected to bring out numerous promising effects in developing the mass-production process of multi-level MEMS. In addition, extrapolation of this planarization method to other materials might reveal important keys to successful process design for ultra-compact, multifunctional, and highly integrated electronic devices, thus reducing their production cost and time. Ongoing work is focusing on more in-depth optimization of poly-Si CMP process to shed light on the planarization of metal layers.

References

[1] R. Jin, S. Li, S. Fang, and F. Redeker, "Proven practice and future application of polysilicon CMP in IC fabrication," in *Proc. Semi IC Seminar*, Taipei, Taiwan, 1998, pp. 263-274.

[2] S. Park, S.-H. Yoon, H. Kim, and H. Jeong, "A hybrid polysilicon planarization for suppressing dishing defects," *J. Mater. Process. Technol.*, vol. 212, no. 12, pp. 2635-2641, 2012.

[3] A. A. Yasseen, N. J. Mourlas, and M. Mehregany, "Chemcial-mechanical polishing for polysilicon surface micromachining," *J. Electrochem. Soc.*, vol. 144, no. 1, pp. 237-242, 1997.

[4] D. Maier-Schneider, A. Köprülülü, S. B. Holm, and E. Obermeier, "Elastic properties and microstructure of LPCVD polysilicon films," *J. Micromech. Microeng.*, vol. 6, no. 4, pp. 436-446, 1996.

[5] D. Maier-Schneider, J. Maibach, E. Obermeier, and D. Schneider, "Variations in Young's modulus and intrinsic stress of LPCVD-polysilicon due to high-temperature annealing," *J. Micromech. Microeng.*, vol. 5, no. 121, pp. 121-124, 1995.

[6] P. French, "Polysilicon: A versatile material for microsystems," *Sens. Actuators A, Phys.*, vol. 99, no. 1-2, pp. 3-12, 2002.

[7] H. Jeong, B. Park, H. Lee, H. Kim, H. Seo, G. Kim, K. Park, M. Kinoshita, and J. Park, "Monitoring system in CMP process," in *Proc. 1st Pac-Rim-CMP*, Tokyo, Japan, 2004, pp. 57-68.

[8] B. D. Tang, X. Xie, and D. S. Boning, "Damascene chemical mechanical polishing characterization and modeling for polysilicon microelectromechanical systems structures," *J. Electrochem. Soc.*, vol. 152, no. 7, pp. G582-G587, 2005.

Sungmin Park received the B.S. degree in mechanical engineering from Pukyong National University, Republic of Korea, in 2002, the M.E. degree in mechanical engineering from University of California at Berkeley, USA, in 2010. He is currently pursuing the Ph.D. degree in mechanical engineering at Inha University, Republic of Korea. He was a researcher in University of Maryland at College Park from 2011 to 2012 and a senior researcher in semiconductor division, Samsung electronics, Republic of Korea from 2013 to 2015. His research activities are focused on bioinspired engineering as well as human-machine interface (HMI) using microfabrication.

Haedo Jeong is a professor at the Pusan National University, Busan, Korea. He received his BS in production engineering in 1987 from the Pusan National University, Busan, Korea. He received his MS in precision mechanical engineering in 1989 from the Korea Advanced Institute of Science and Technology, Daejeon, Korea. He received his PhD in mechanical and precision engineering in 1994 from the Japan Tokyo University, Japan. Research interest is chemical mechanical planarization, polishing pad, and grinding.

Sang-Hee Yoon received the B.S. degree in mechanical design and production engineering from Yonsei University, Republic of Korea, in 2001, the M.S. degree in mechanical engineering from Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea, in 2003, and the Ph.D. degree in mechanical engineering from University of California at Berkeley, USA, in 2010. He joined Inha University, Republic of Korea, in 2013 and is currently an assistant professor in the Department of Mechanical Engineering and a director of micro/nano soft biomechanics laboratory. He was a researcher in agency for defense development, Republic of Korea, from 2003 to 2007, and a postdoctoral fellow in Harvard University, USA, from 2010 to 2012. His research interests are in design, modeling, and fabrication of biological model systems to advance understanding of body mechanics, bioinspired engineering for biomedical applications, and human-machine interface (HMI) in hopes of developing machines communicable with human.