A Study on Hot Carrier Reliability of Radiation Hardened H-gate PD SOI NMOSFET after Gamma Radiation

Jinghao Zhao, Xuefeng Yu, Jiangwei Cui, Qiwen Zheng, Hang Zhou, and Qi Guo

Abstract—**Reliability of space applied micro/nanometer devices are simultaneously facing space radiation environment and own reliability issues such as HCI（hot carrier injection）effect. To clarify the effect of mature RH (radiation hardened) technology for deep submicron device on its hot carrier reliability, the author performed gamma irradiation and hot carrier stress on RH H-Gate PD (partially depleted) SOI NMOS and commercial strip-shaped gate PD SOI NMOS as control group. He makes a detailed analysis on hot carrier reliability and reaches a conclusion that compared to irradiated strip-shaped gate devices, HCI effect is partly improved in irradiated RH H-gate. On the other hand, in comparison with unirradiated RH H-gate devices, there's still enhanced HCI degradation in irradiated ones. Mechanism is explained as the coupling effect between front gate and back gate caused by TID (total ionizing dose effect) induced charge trapping in buried oxide.**

Index Terms—**Reliability, NMOS, hot carrier injection, total dose effect.**

I. INTRODUCTION

With the development of semiconductor technology and feature size scaling down to nanometer level, hot carrier effect becomes a more serious reliability issue. Therefore, for micro-nano device on spacecraft, its reliability simultaneously faces radiation environment and its own hot carrier effect [1], [2].

Essentially speaking, TID and HCI are both the physical processes that oxide and interface trap charges are induced into Si-SiO2 system, affecting device's working parameters. As early as 1986, Pro. Fleetwood from Vanderbilt University raised that space device ought to possess not only radiation resistance but also high reliability. He pointed that electrical parameters influenced by TID and HCI were roughly identical and assumed that two kinds of damage would be eliminated in the future [3].

So far research about TID and HCI effects of SOI has been reported a lot. Padova University, Institute of Microelectronics Barcelona and Interuniversity Microelectronics Centre have successively reported that TID radiation strengthen hot electron trapped phenomenon and enhance the HCI effect of SOI device [4], [5].

However, there's few reports about hot carrier reliability of radiation hardened devices. National Tsing Sua University found that hot carrier reliability and radiation resistance of MONOS were both improved by irradiation-then-anneal treatments [6]. Arizona State University had a research on RH annular gate MOSFET and reached the conclusion that RH process extended hot carrier lifetime in contrast to conventional geometry design [7].

HCI effect and TID show similar mechanism in damage to MOSFETs. But TID brings uniform damage to the channel while damage induced by HCI is mainly focused on the drain end of the channel. Furthermore, because of existence of buried oxide in SOI devices, mechanism of TID is more complicated. It's fair to doubt whether TID induced HCI enhancement is restrained in RH SOI, same as previous conclusions in RH bulk MOSFETs.

In this contribution, 130nm RH H-gate PD SOI NMOSFETs are irradiated to 300krad (Si) and performed 3000s hot carrier stress. To analyze effect of RH process on device's characteristics, commercial strip-shaped gate PD SOI NMOSFETs is submitted the same experimental process for comparison. The degradation of electrical parameters during radiation and stress is evaluated, and the mechanisms responsible for the observed phenomena are discussed.

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II. EXPERIMENTAL DETAILS

130nm H-gate PD SOI NMOSFETs fabricated with silicon ion implantation RH process and SIMOX (separation by implantation of oxygen) material is employed as experimental samples. The samples are with a 100nm thick top Si film and a 145nm thick BOX. The devices are 24-pin DIP packaged. The operating voltage is 3.3V and gate oxide thickness is 6.8nm. W/L is selected as 10/0.35. The commercial strip-shaped gate PD SOI is with the same parameters except process and structure. Cross sections of samples are shown as Fig. 1. Before irradiation, DC characteristics of samples were measured.

Irradiation experiment was carried out in Xinjiang Technical Institute of Physics and Chemistry, the Chinese Academy of Sciences. ^{60}Co was chosen as radiation source. The dose rate is 100rad(Si)/s and the total dose is 300krad(Si).

Two kinds of devices were both biased with ON bias during radiation.

After irradiation, samples were annealed for 168h at 20℃. Then hot carrier stress was performed for 3000s. During hot carrier test, the drain voltage was kept as 3.63V, which is corresponding to 110% operating voltage. The gate voltage was chosen as the voltage corresponding to maximum of body current in I_{body} -V_G curve. Other pins were grounded. Six points in time including 1, 10, 100,300,1000, 3000s were selected to pause electrical stress for parameter test. There were also samples experienced same experimental procedure but no irradiation and annealing. All the electrical tests were measured with Keithley 4200B semiconductor test system at room temperature.
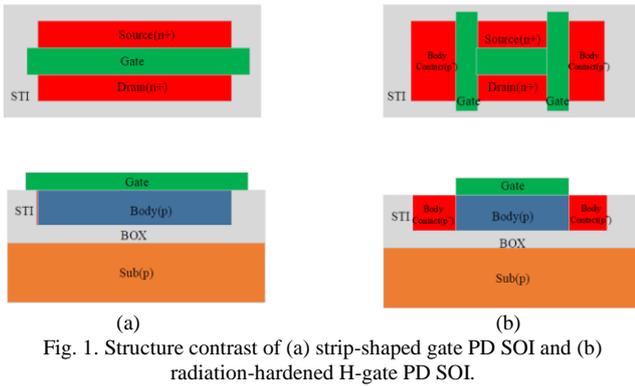

Fig. 1. Structure contrast of (a) strip-shaped gate PD SOI and (b) radiation-hardened H-gate PD SOI.

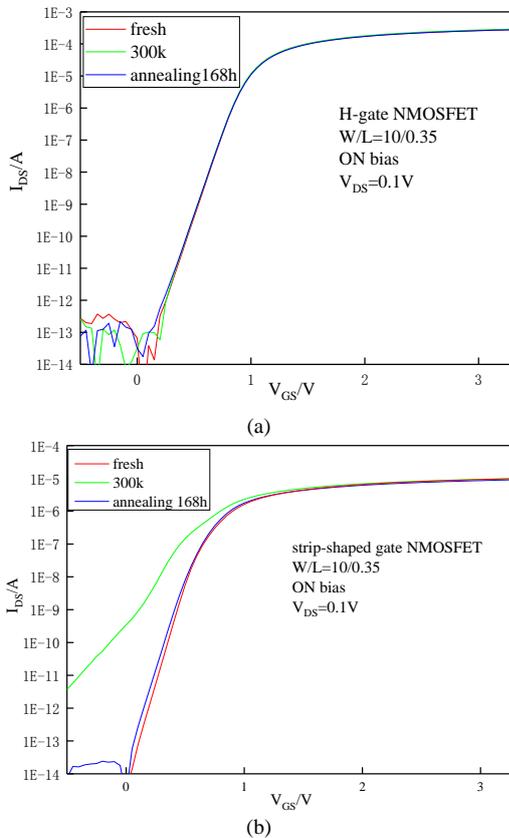## III. RESULTS AND DISCUSSION

(a)

(b)

Fig. 2. TID response of PD SOI NMOSFETs front gate under ON bias transfer characteristics at various periods (a)H-gate (b)strip-shaped gate.

As Fig. 2 shown, no significant change in off state leakage current and threshold voltage shift is observed in RH H-gate

devices' front gate transfer characteristics after irradiation for RH process and avoiding the effect of shallow trench isolation (STI), in which oxide trap charge would be induced under TID radiation. Compared to the obvious VT shift in strip-shaped gate devices after irradiation, RH H-gate have effective radiation resistance to TID effect on front gate.
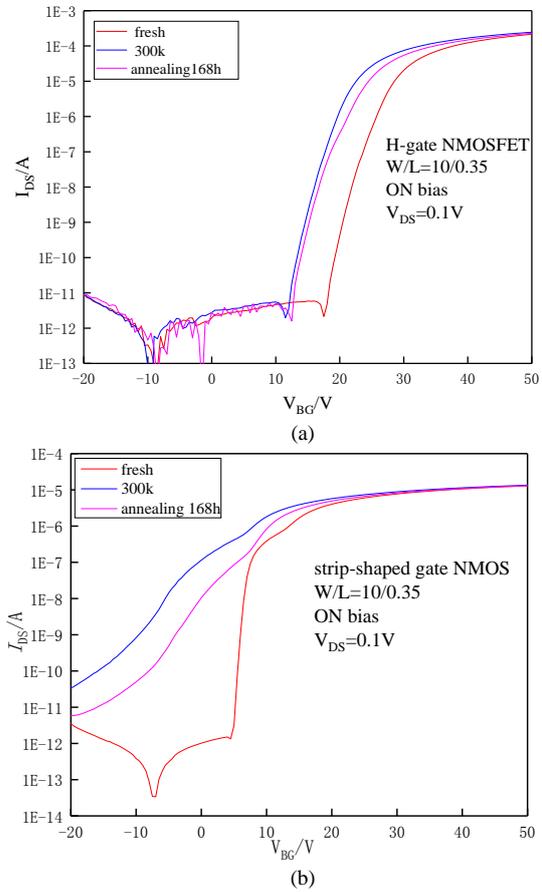

(a)

(b)

Fig. 3. TID response of PD SOI NMOSFETs back gate under ON bias transfer characteristics at various periods (a)H-gate (b)strip-shaped gate.

As shown in Fig. 3, there still exists negative shift in irradiated RH H-gate back gate characteristics. But gate doesn't open when back gate voltage is 0V. And compared to strip-shaped gate, no significant off state leakage current is observed in irradiated RH H-gate back gate. RH process also makes achievement in PD SOI back gate transfer characteristics.

Silicon ion implantation process applied in RH H-gate SOI generates electron traps, which trap electrons and neutralize TID induced oxide trapped charge [8]. And improved SIMOX process reduces both interface trapped charge and oxide trapped charge [9]. Meanwhile, H shaped gate declines the effect of STI, in which TID radiation may induce charge trapped and cause off state leakage current as shown in Fig. 4. So leakage current and threshold voltage shift in RH H-gate front gate are not obvious. Transfer characteristics of back gate has been improved a lot. However, there still exists threshold shift, which demonstrates that interface trapped charge in buried oxide.

GM is an electrical parameter closely related to carrier mobility. It can be drawn form Fig. 5 there is no remarkable change in subthreshold region of RH H-gate. Increment percent after irradiation of transconductance maximum of

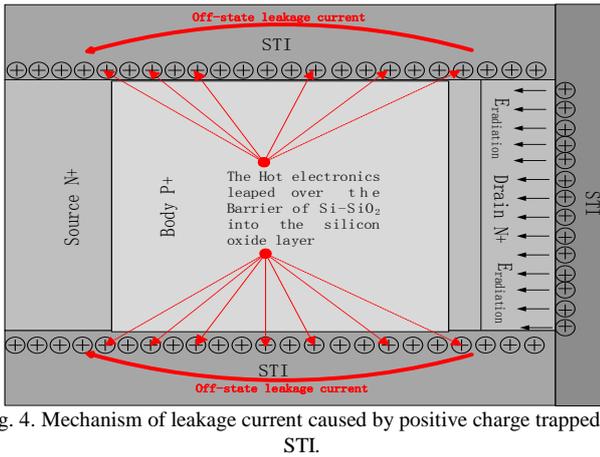H-gate is 2.55% and the strip-shaped gate is 6.18%.

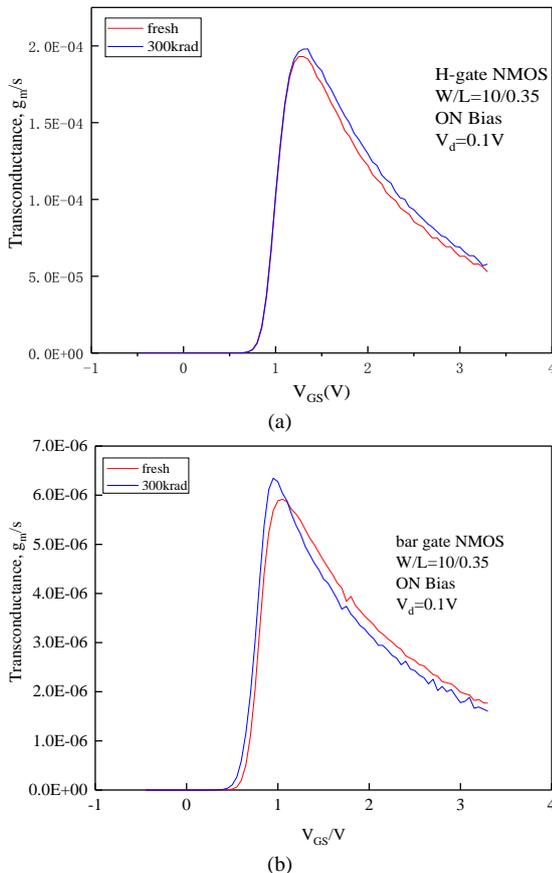Fig. 4. Mechanism of leakage current caused by positive charge trapped in STI.

(a)

(b)

Fig. 5. GM of PD SOI before and after irradiation(a)H-gate (b)strip-shaped gate.

As the dominated factor of hot carrier injection in conventional environment, body current is measured as Fig.6 shown. Maximum of Ibody of H-gate and trip-shaped gate samples decline 19.4% and 3.84% respectively. From degradation of irradiated samples, no obvious improvement is investigated in RH devices.

Body current is considered as a judging factor in conventional MOSFET reliability test [10] while there's no obvious difference between body current degradation degree of H-gate and strip-shaped gate in Fig. 6. It's due to the buried oxide. In normal MOSFET, essentially, body current originates from hot carrier induced by channel drain side, hot electron is injected into gate oxide while hot hole is collected as body current. For SOI devices, compound effect of

recombination center at Si——buried oxide and back gate channel electron needs to be taken into consideration. Collected hot hole is no longer judgement factor of body current. So in this article, linear saturated current is used to characterize hot carrier degradation degree of PD SOI.
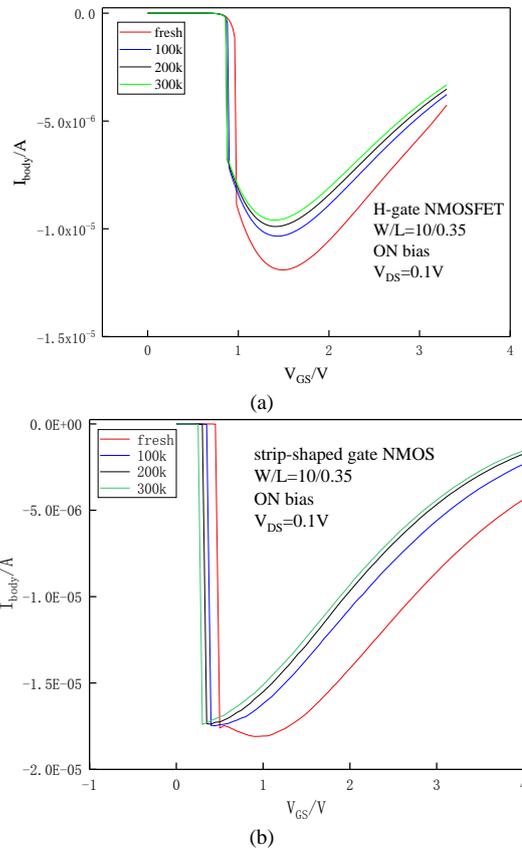

(a)

(b)

Fig. 6. Body current versus the VGS at different total levels for PD SOI NMOS (a)H-gate (b)strip-shaped gate.

In Fig. 7, linear coordinate replaces logarithmic coordinate to characterize degradation of linear saturated current more easily. It can be seen that Idlin obviously decreases after 3000s hot carrier stress. During hot carrier stress, degradation percent of Idlin is measured as Fig. 8 shown. Compared to strip-shaped gate, hot carrier reliability of irradiated RH H-gate partly improves. But there still exists TID induced HCI enhancement effect as strip-shaped gate devices. As Fig.9 shown, degradation during electric stress of GM maximum of irradiated RH H-gate is slighter than strip-shaped gate.
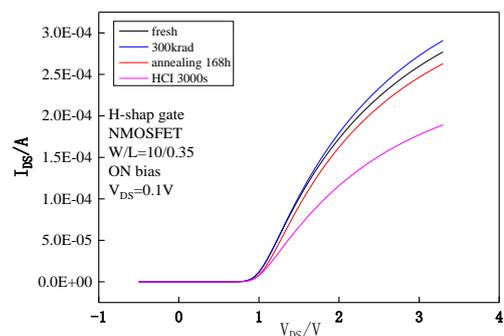

Fig. 7. Linear saturated current of RH H-gate PD SOI at different times.

During hot carrier test, applied electric stress causes energetic electrons or holes that can be injected into the oxide

and become oxide-trapped charge, create interface traps by breaking the silicon-hydrogen bonds near Si-SiO2 interface. The dominant degradation is interface trap generation near the drain end of the channel which is mainly caused by high electric field in pinch-off region of devices [11]. The reaction associated with the formation of interface traps can be shown as

$$\Xi \; Sis\text{-}H + e\text{-} \rightarrow Si^* + Hi \tag{1}$$
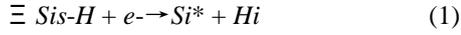
Si_s is a surface silicon atom, Hi is a interstitial hydrogen atom, and Si^* is represents the interface trap or silicon dangling bond. To break the *Si-H* bond and form an un-passivated silicon dangling bond such as interface trap, the hot-carrier (hole or electron) must have an energy of approximately 3.5eV or greater. The value of energy required is determined by summing the energy of the Si-H bond (0.3eV) and barrier energy (3.2eV) [12]. To summarize, for SOI devices, the dominant degradation mechanism is due to interaction between hot carrier and dangling bonds at the gate oxide/silicon interface.
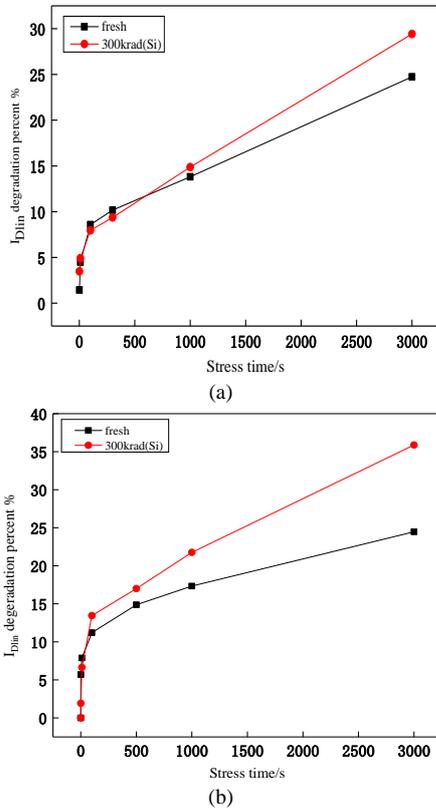

Fig. 8. Linear degradation percentage during hot carrier stress of irradiated and unirradiated (a)H-gate and (b)strip-shaped gate.

It is worth noting in Fig. 7 that Idlin goes up after 300krad(Si) radiation. Nevertheless, to the best of our knowledge, in bulk silicon devices, TID radiation causes degradation of transconductance and Idlin, resulting in the decline of driving ability. In linear region, Idlin could be described as the formula:

$$I_{DS} = \frac{W}{L} \bullet \mu \bullet \mathrm{C_{ox}} \left(V_{GS}\text{-}V_T\text{-}\frac{V_{DS}}{2} \right) V_{DS} \tag{2}$$

μ is the carrier mobility of channel. Cox is the gate oxide capacitance per unit. In Fig. 7, variable electrical parameters

which could affect channel current are only carrier mobility and threshold voltage. Interface trapped charge in the channel induced by TID radiation strengthens the electron scattering and reduces the carrier mobility. So there must be a significant effect negative of VT on Idlin. However, due to the radiation hardened process, there are only a small amount oxide trapped charges trapped in front gate. It can be inferred as the effect of charge trapped in back gate. To analyze the combination effect between front gate and back gate further, degradation percentage of GM$_{max}$ during hot carrier stress is measured as Fig. 9. As illustrated in Fig. 9, degradation percentage of GM$_{max}$ of irradiated H-gate samples and unirradiated ones after 3000s hot carrier stress is 34% and 30%. Radiation induced small amount oxide trapped charges in front gate is annealed by the hot carrier stress, so the difference between two groups could be considered as the effect of the back gate.
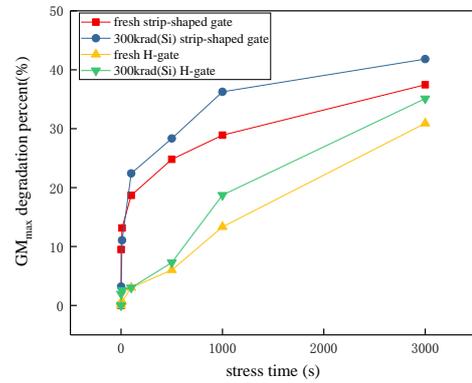

Fig. 9. Degradation percentage of GMmax during hot carrier stress of irradiated and unirradiated H-gate and strip-shaped gate.
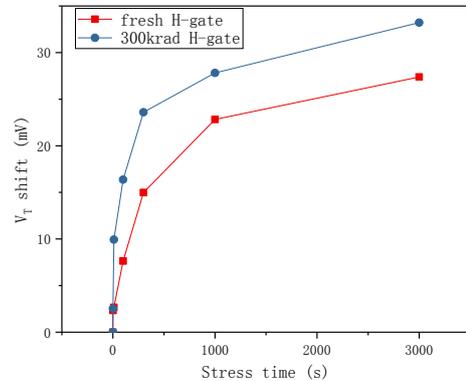

Fig. 10. Threshold voltage shift of H-shaped gate PD SOI during hot carrier stress.

It can be attributed as Fig. 11 that positive charges are trapped below junctions region under the electrical field, which locates below the reverse biased Source/Box and Drain/Box junction. In the Si film, the both sides near source and drain terminal is fully depleted, and the center part in the body region will keep neutral [10], [13]. And coupling degree between front gate and back gate increases with accumulation of total dose. Thus it can be easy to explain enhanced HCI effect in RH H-gate SOI. On one side, due to radiation lowering the potential barrier of the parasitic source-to-body diode, more hot electron can be injected into gate oxide, causing more interface defects. On the other side, because of the interface damaged by radiation, Si-H dangling bonds can be more vulnerable to be broken during hot carrier stress.

Therefore, as Fig. 8 shown, mobility of carrier in irradiated H-gate device is with more severe degradation.

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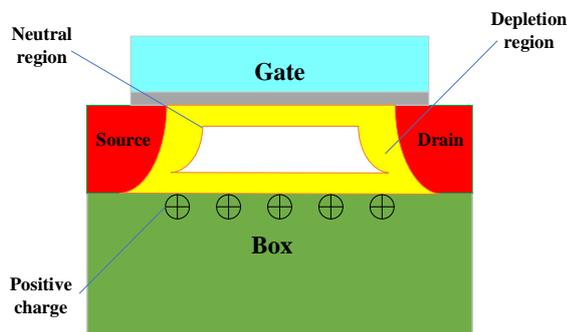

Fig. 11. TID radiation induced coupling effect of PD SOI NMOSFETs.

To sum up, there's partly improvement in RH H-gate hot carrier reliability under radiation environment. But TID induced HCI enhancement has been not completely eliminated due to the coupling effect between front gate and back gate caused by trapped positive charge at the interface of buried oxide and body region.

IV. CONCLUSION

This paper has performed a study on hot carrier reliability of RH H-gate PD SOI NMOSFETs. Based on the experimental results, it is investigated that though hot carrier reliability is partially improved, enhanced HCI effect still exists in RH H-gate devices. Interface traps induced by TID cause a coupling effect between front gate and back gate and make hot carrier reliability of front gate affected by buried oxide. In order to strengthen radiation resistance and hot carrier reliability of H-gate PD SOI simultaneously, process of improving quality of Si-buried oxide interface and reducing quantity of Si-H dangling bonds to restrict the generation of interface traps.

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