Comparison study of Dual Material Gate Silicon on Insulator junctionless Transistor and with Junction Transistor for Analog Performance

S. C. Wagaj and S. C. Patil

***Abstract*—In this paper compare analog performance parameters of dual material gate silicon on Insulator iunctionless transistor (DMG SOI JLT) and DMG SOI Transistor. In this paper analog parameters as like transconductance (g_m), transconductance generation factor (gm/I_{DS}), output conductance (g_d), intrinsic gain (g_m/g_d) , intrinsic gate delay, intrinsic static power dissipation and cut off frequency. It has been observed that transconductance, transconductance generation factor, output conductance, intrinsic gain, intrinsic gate delay, intrinsic static power dissipation and cut off frequency of DMG SOI JLT improved by 12%, 29%, 69%, 21%, 5%,26% and 3% respectively over the DMG SOI Transistor. It has been observed that due to work function difference of dual material gate improves the electrostatic control on channel and on current also improved by 34% over the DMG SOI Transistor. The DMG SOI JLT is the best candidate for low power device performance.**

***Index Terms*—Dual material gate, junctionless transistor, intrinsic delay, silicon on insulator.**

I. Introduction

According to international technological road map for semiconductors (ITRS) channel length of MOSFET decreases up to 20nm. However, short channel effect (SCE) problem and analog performance parameters improvement is very challenging in front of researchers. Silicon on insulator technology superior electrical characteristics compare to bulk technology such as less junction capacitance, increase mobility, excellent latch up immunity and short channel effect [1]. In nanoscale metal oxide semiconductor field effect transistor (MOSFET) leakage current increases due to charge sharing effect because source and drain close with each other.

However, shallow source and drain formation is very difficult to manufacturer. Dual material gate in bulk MOSFET transconductance enhancement and suppression of short channel effect due to step function in channel potential [2]. In DMG n-channel MOSFET $\Phi_{M1}>\Phi_{M2}$ (Φ_{M1} is workfunction of gate material 1 and Φ_{M2} is workfunction of gate material 2) and vice versa for p-channel MOSFET [3]-[5]. Dual material gate (DMG) structure in a fully depleted SOI MOSFET leads to subdued SCE due to a step-function in the channel potential profile. The shift in the surface channel potential minima position is negligible with increasing drain biases. The electric field in the channel at the drain end is also reduced leading to reduced hot-carrier effect. Also, the variation of the minimum channel potential with decreasing thin-film thickness can be more effectively reduced in the DMG structure at shallow thin-film thicknesses [6].

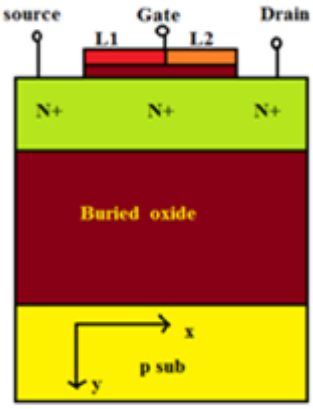

Fig. 1. Schematic of DMG SOI JLT structure.

Some authors demonstrated that the dual material double gate (DMDG) structure (channel length 100nm) leads to reduced SCEs, as the surface-potential profile shows a step at the interface of the two materials of the front gate, which reduces drain conductance and DIBL. Due to the discontinuity in the surface potential of the DMDG structure, the peak electric field at the drain is reduced substantially, by approximately 40%, when compared with that of the double gate (DG) structure that leads to a reduced hot carrier effect.

Junctionless with uniform doping of channel overcome these challenge. Uniform channel doping of junctionless transistor fabrication is very simple. Perpendicular electric field on channel is very low when MOSFET is in ON state. Junctionless device have full CMOS functionality. They have minimum subthreshold slope, extremely low leakage current and less degradation of mobility with gate voltage [6]-[9]. Haijun Lou et al demonstrate dual material gate junctionless nanowire transistor [10]. It has been observed that transconductance is very low below 0.06mS at channel length 40nm. In this paper below 40nm channel length results not observed. Ratul k Baruah et al demonstrate dual material gate junctionless transistor with spacer have gate capacitance is 1.2fF at V_{GS} is 0.8V and cut off frequency is 225GHz [11]-[16]. It has been observed that cut off frequency is low and gate capacitance is high. I already publish paper on dual material gate silicon on nothing and silicon on insulator

Manuscript received October 23, 2018; revised May 1, 2019.

The authors are with JSPM's Rajarshi Shahu College of Engineering, Pune Savitribai Phule Pune University, Pune, India (e-mail: scwagaj@yahoo.com, shailaja.rscoe@gmail.com).

doi: 10.18178/ijmmm.2019.7.3.448

junctionless transistor [17], [18], but cut off frequency, gate capacitance and intrinsic gain not studied. In this paper simulated result of different parameters as like transconductance, transconductance generation factor, output conductance, intrinsic gain, intrinsic gate delay and cut off frequency of DMG SOI JLT compare with DMG SOI transistor.

II. Device Structure and Simulation

Simulated result discusses here using COGENDA TCAD software, in this software contents mathematical model. 1) High field mobility 2) Impact ionization 3) Band to band tunneling 4) carrier trapping and Lombardi mobility model incorporate in this model. Channel length 20nm, oxide thickness t_{ox}=1nm, channel thickness t_{si}=10nm. Gate material 1 is p-poly material and gate material2 is n-poly material.

TABLE I: Parameters of DMG SOI Junctionless and with Junction Transistor.

Sr.No.	Parameters	Symbols	Unit	Parameter value
1	Physical gate length1	L_G	nm	Variable
1	Physical gate length2	L_G	nm	Variable
2	Gate oxide thickness	T_{ox}	nm	1
3	Channel thickness	T_{si}	nm	10
4	Buried oxide thickness	T_{box}	nm	360
5	Doping density	N_D	cm^{-3}	0.4×10^{18}
6	Supply voltage	V_{DD}	V	1
7	Substrate doping		cm^{-3}	1×10^{16}
8	Source and drain doping		cm^{-3}	1×10^{19}
9	Gate 1 work function	L_1	eV	5.2
10	Gate 2 work function	L_2	eV	4.2

Lombardi Surface Mobility Model

The Lombardi mobility model [19] is an empirical mobility model shown in equation 1. The mobility model consist three different components as like surface roughness, phonon scattering and doping dependent mobility model.

Bulk mobility model in Lombardi mobility model is similar to musette's model.

$$\mu_b = \mu_0 \exp\left(-\frac{P_c}{N_{tot}}\right) + \frac{\mu_{max}-\mu_0}{1+\left(\frac{N_{tot}}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1+\left(\frac{C_s}{N_{tot}}\right)^{\beta}} \quad (1)$$

$$\mu_{max} = \mu_2\left(\frac{T}{300}\right)^{\xi}$$

$$\alpha = 0.680, \beta = 2.0, \xi = 2.5, \mu_0 = 52.2cm^2/v.s, \mu_2 = 1417cm^2/v.s,$$
$$C_S = 3.43\times10^{20}cm^{-3}, C_r = 9.68\times10^{16}cm^{-3}$$

Carrier recombination, generation model, Fermi Dirac statics and impact ionization models and Lombardi mobility model in COGENDA TCAD. The quantum confinement model also have been incorporated in the simulation.

III. Results and Discussion

The characteristics of analog parameters compare of DMGSOI junctionless and with junction Transistor.

Table II contents transconductance values of DMG SOI junctionless and with junction transistor.

TABLE II: Transconductance Values of DMG SOI Junctionless and with Junction Transistor

L_G (nm)	DMG SOI JLT		DMG SOI Transistor	
	g_m (S) at $V_{GS}=V_{DS}$= 1V	g_m (S) at V_{DS}=0.5V,I_D=5μ A	g_m (S) at $V_{GS}=V_{DS}$=1 V	g_m (S) at V_{DS}=0.5V,I_D =5uA
20	7.03×10-5	8.61 ×10-5	4.79 ×10-6	7.11 ×10-5
30	7.66 ×10-6	6.5 ×10-5	1.684 ×10-5	7.3 ×10-5
40	1.06 ×10-4	7.9 ×10-5	11.4 ×10-4	7.6 ×10-5

Fig. 1 shows the transconductance g_m ($=\partial I_D/\partial V_{GS}$) indicate how well device convert voltage to current. Gate material work function is different then step potential generate. Due to step potential in the channel g_m increases. Electron velocity increases in the channel due to workfunction difference, high workfunction at source side and low workfunction of gate material at drain side. Due to high peak electric field at source side electron velocity increases, then transconductance of MOSFET increases. DMG SOI JLT transconductance is 0.07mS at channel length is 20nm.

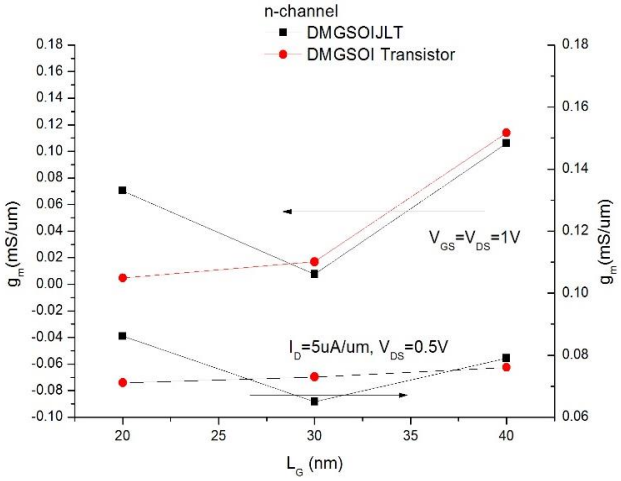

Fig. 1. Transconductance g_m v/s channel length.

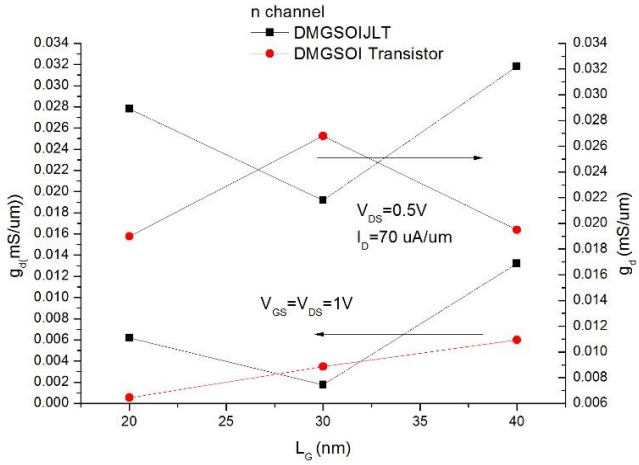

Fig. 2. Output conductance v/s channel length.

Fig. 2 shows output conductance g_d compare at different channel length of DMG SOI junctionless and with junction. It has been observed that output conductance of DMG SOI JLT

is maximum at channel length is 20nm and 40nm. Output conductance of DMG SOI JLT is 6.18μS and DMG SOI Transistor is 8.51μS at V_{GS}=V_{DS}=1V.

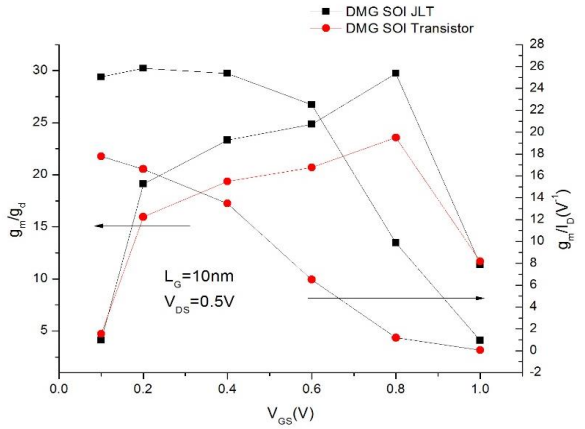

Fig. 3. Intrinsic gain and transconductance generation factor versus gate voltage for DMG SOI JLT and with junction.

TABLE III: OUTPUT CONDUCTANCE G_D OF DMG SOI JUNCTIONLESS AND WITH JUNCTION TRANSISTOR

L_G (nm)	DMG SOI JLT		DMG SOI Transistor	
	g_d (S) at V_{GS}=V_{DS}=1V	g_d (S) at V_{DS}=0.5V, I_D=7μA	g_d (S) at V_{GS}=V_{DS}=1V	g_d (S) at V_{DS}=0.5V, I_D=7μA
20	6.18 ×10-6	2.89 ×10-5	5.5 ×10-7	8.51 ×10-6
30	1.76 ×10-6	2.18 ×10-5	3.48 ×10-6	2.68 ×10-5
40	1.32 ×10-5	3.22 ×10-5	6.01 ×10-5	19.5 ×10-5

Table III contents output conductance values g_d at different channel length.

Table IV contents values of g_m/I_{DS} and g_m/g_d of DMG SOI JLT and with junction transistor. The g_m/I_{DS} is another important parameter in analog parameters and g_m/I_{DS} indicate efficiency of device how to convert dc power into ac frequency and gain performance as shown in Fig. 3. The g_m/I_{DS} is maximum at device in subthreshold region means OFF current is minimum. g_m/I_{DS} of DMG SOI JLT is 25 and 18 is DMG SOI Transistor.

TABLE IV: THE G_M/I_{DS} AND G_M/G_D OF DMG SOI JLT AND DMG SOI TRANSISTOR

Sr.No.	V_{GS} (V)	g_m/I_{DS} (V^{-1}) DMG SOI JLT	g_m/I_{DS} (V^{-1}) DMG SOI T	g_m/g_d DMGSOIJLT	g_m/g_d DMG SOI T
1	0.1	25.04679	17.77271	4.114907	4.70745
2	0.2	25.82012	16.61642	19.10714	15.9531
3	0.4	25.37287	13.46869	23.32455	19.37122
4	0.6	22.51411	6.508871	24.84093	20.7147
5	0.8	9.863399	1.185213	29.73523	23.5841
6	1	0.941379	0.061284	11.37702	11.68293

TABLE V: CUT OFF FREQUENCY COMPARISON OF DMG SOI JUNCTIONLESS AND WITH JUNCTION TRANSISTOR

Sr.No.	V_{GS} (V)	Cut off frequency DMGSOIJLT (GHz)	V_{GS} (V)	Cut off frequency DMG SOI Transistor(GHz)
1	0.7	204	0.4	114
2	0.8	398	0.6	402
3	0.9	418	0.7	368
4	1	163	0.8	170

In subthreshold region g_m/I_{DS} of DMG SOI JLT is 25.04 and DMG SOI Transistor value is 17.77. Smaller value of subthreshold current its higher value of g_m/I_{DS} in subthreshold region. The g_m/I_{DS} of DMG SOI JLT is 29% minimum value compare to DMG SOI Transistor at MOSFET in subthreshold region.

Table V contents cut off frequency at different V_{GS}.

In Fig. 4 shows that cut off frequency characteristics of the DMG SOI JLT and DMG SOI Transistor are shown. The delimitation of the unity gain cut off frequency f_t. The DMG device exhibits higher f_t when V_{GS} is small due to higher g_m compared with DMG SOI Transistor. At a maximum V_{GS}, the advantage of higher f_t in the DMG SOI JLT. The maximum f_t of the DMG SOI JLT is 418GHz which is 3% improvement compared with DMG SOI Transistor counterparts. Fig.5. shows that intrinsic gate delay and static power dissipation of DMG SOI junctionless and with junction at different channel length.

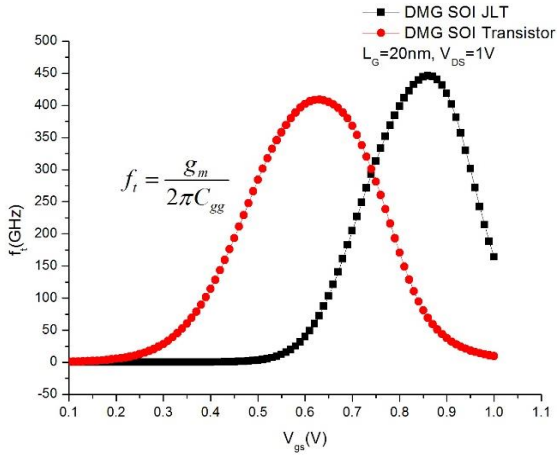

Fig. 4. Cut off frequency f_t as a function of V_{GS}.

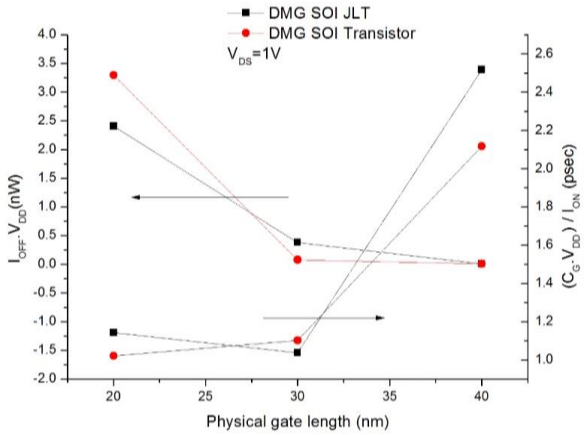

Fig. 5. Intrinsic gate delay and static power dissipation variation with physical gate length at V_{DS}=1V.

The intrinsic static power dissipation ($I_{OFF}.V_{DD}$) and the intrinsic gate delay ($C_G.V_{DD}/I_{ON}$) are the useful design parameters for digital logic circuit. C_G is the gate capacitance which is normally sum of gate-to-source C_{GS} and gate-to-drain C_{GD}. $C_G.V_{DD}/I_{ON}$ in the proposed DMGSOIJLT device does affect the operating speed of logic circuit based on this device. Since $I_{OFF}.V_{DD}$ and $C_G.V_{DD}/I_{ON}$ of a MOSFET indicates both power dissipation and delay, DMG SOI JLT is best candidate for design CMOS circuits. Table VI contents values of intrinsic gate delay and static power dissipation.

The 26% improvement in intrinsic static power dissipation of DMG SOI JLT at channel length 20nm. This device is best

candidate for low power analog CMOS circuit design. Fig. 6 shows that drain current variation versus gate voltage of DMG SOI JLT at different channel length 20nm, 30nm and 40nm. It has been observed that channel length decreases drain current increases but off current decreases when channel length increases. In p channel DMG SOI JLT work function of gate material is n-poly material its work function is minimum and gate material at drain side is p-poly material its workfunction is maximum. Threshold voltage of p channel DMG SOI JLT decreases when channel length increases. Fig.7 shows that drain current versus gate voltage of n and p channel DMG SOI JLT and DMG SOI with junction at channel length 20nm and V_{DS} is 1V. It has been observed that n channel DMG SOI with junction current driving capability is maximum as compared to n channel DMG SOI JLT due to workfunction difference of gate material. DMG SOI JLT current driving capability is minimum because more doping density in channel region.

TABLE VI: INTRINSIC GATE DELAY AND STATIC POWER DISSIPATION VALUES OF DMG SOI JUNCTIONLESS AND WITH JUNCTION TRANSISTOR

L_G (nm)	I_{OFF} . V_{DD} (nw)		C_G . V_{DD}/I_{ON} (psec)	
	DMG SOI JLT	DMG SOI Transistor	DMG SOI JLT	DMG SOI Transistor
20	2.41	3.30	1.14	1.02
30	0.38	0.078	1.04	1.10
40	0.008	0.00646	2.52	2.12

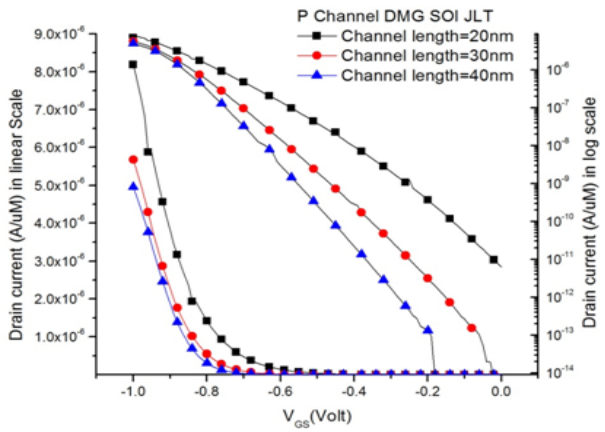

Fig. 6. Drain current versus gate voltage of n and p channel DMG SOI JLT.

High doping density in channel region, ionization scattering of electron increases and mobility of electron degrade. Mobility degradation is maximum due to ionization scattering in DMG SOI JLT as compared to mobility degradation due surface scattering in DMG SOI with junction. It has been observed that off current of DMG SOI JLT is minimum as compared to DMG SOI with junction due to high workfunction of gate material of DMG SOI JLT. More depletion of channel due to high work function of gate material, hence off current is minimum.

The characteristics of DMG SOI JLT are investigated and compared with a corresponding compatible DMG SOI Transistor.

Table VII shows that drain current values at different gate voltage DMG SOI JLT and DMG SOI Transistor.

In Fig. 7 all result observed at band-to-band tunneling model. In junctionless transistor band to band tunnel current is maximum as compared to with junction transistor. Threshold voltage of DMG SOI JLT is minimum as compared to with junction transistor.

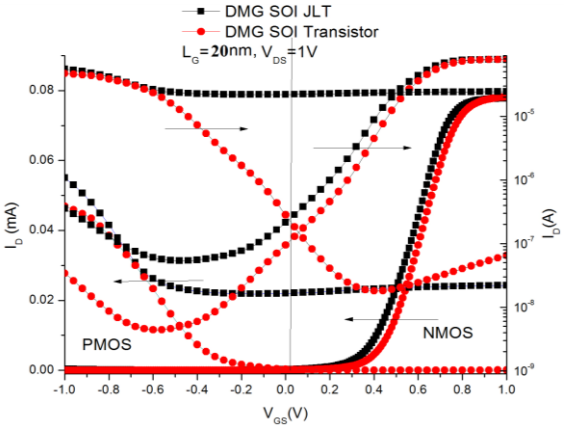

Fig. 7. I_D versus V_{GS} characteristics of n and p channel DMG SOI Transistor and DMG SOI JLT.

TABLE VII: DRAIN CURRENT W.R.T TO GATE TO SOURCE VOLTAGE

Sr.No.	V_{GS}	n-channel DMG SOI JLT	n-channel DMG SOI Transistor	p-channel DMG SOI JLT	p-channel DMG SOI Transistor
		Drain current (A)			
1	-1	3.53×10^{-7}	3.42×10^{-8}	5.50×10^{-5}	4.69×10^{-5}
2	-0.9	2.16×10^{-7}	1.71×10^{-8}	4.93×10^{-5}	4.41×10^{-5}
3	-0.6	5.99×10^{-8}	4.42×10^{-9}	3.25×10^{-5}	3.16×10^{-5}
4	-0.3	6.18×10^{-8}	9.58×10^{-9}	2.37×10^{-5}	1.44×10^{-5}
5	0	2.13×10^{-7}	9.51×10^{-8}	2.20×10^{-5}	2.82×10^{-7}
6	0.1	4.39×10^{-7}	2.04×10^{-7}	2.22×10^{-5}	9.99×10^{-8}
7	0.5	4.37×10^{-5}	3.58×10^{-5}	2.35×10^{-5}	1.97×10^{-8}

Fig. 7 shows that drain current v/s gate voltage at V_{DS}=1V and channel length is 20nm. The n-channel and p-channel DMG SOI JLT ON current is maximum compare to n and p channel DMG SOI Transistor at V_{GS}=0.5V. Junctionless transistor current driving capability increases due to work function difference of gate material. Electron velocity increases due to step potential in the channel, when electron velocity increases then current driving capability increases. Another advantage of junctionless transistor is perpendicular electric field is very low when transistor is in ON state. Perpendicular electric field is very low means mobility degradation decreases.

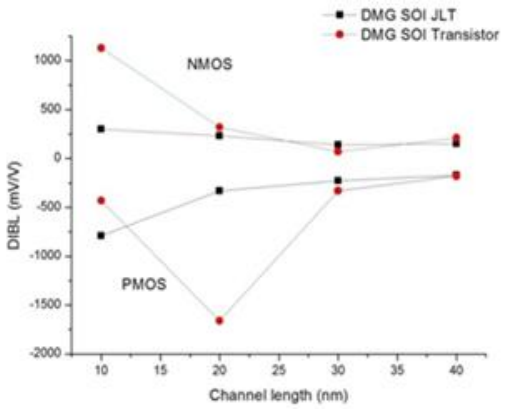

Fig. 8. DIBL versus channel length for different channel length.

Fig. 8 shows that DIBL of DMG SOI JLT and DMG SOI transistor at different channel length. DIBL is calculated by equation (2).

$$DIBL(mV) = \frac{V_{thLin} - V_{thSat}}{V_{dSat} - V_{dLin}} \quad (2)$$

Drain Induced Barrier Lowering means threshold voltage difference when V_{DS}=0.05V and V_{DS}=1V.[DIBL=V_{th} (V_{DS}=0.05V)-V_{th}(V_{DS}=1V)]. DIBL means the reduction of the potential barrier eventually allows electron flow between the source and drain, even if the gate to source voltage is lower than the threshold voltage. DMG SOI JLT's DIBL value is minimum as compared to DMG SOI transistor at channel length 20nm.

TABLE VIII: DIBL AT DIFFERENT CHANNEL LENGTH OF N AND P CHANNEL DMG SOI JLT

Sr.No.	Channel length (nm)	DIBL (mV/V) p-DMG SOI JLT	DIBL (mV/V) n-DMG SOI JLT
1	20	-330	230
2	30	-230	140
3	40	-170	150

Fig. 9 shows that variation of subthreshold slope at different channel length of DMG SOI JLT and DMG SOI transistor.

Subthreshold slope [SS] [20] can be expressed as

$$S = \frac{KT}{q}\ln(10)\left[1 + \frac{1}{C_{ox1}}\left(\frac{C_{si}C_{ox2}}{C_{si} + C_{ox2}}\right)\right] \quad (3)$$

C_{si} is body capacitance and C_{ox1} is gate oxide capacitance and C_{ox2} is buried oxide capacitance. SS is limited by the first term to 60mV/ decade.

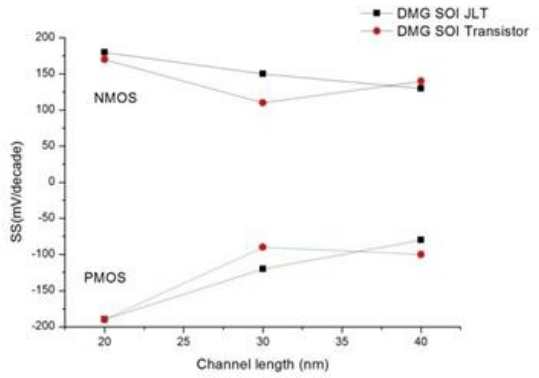

Fig. 9. Variation of Subthreshold swing with physical gate length of n channel and p channel of DMG SOI JLT and DMG SOI Transistor.

Higher SS means that the device can have a fewer orders of change in drain current from the off state to the V_T, which in turn means a higher off current for a given V_T. SS can be made smaller close to 60mV/decade by using thinner gate oxide thickness or lower substrate doping concentration. SS of DMG SOI JLT is minimum as compared to DMG SOI transistor at channel length 40nm. Workfunction of gate material of DMG SOI JLT is 4.77ev. Due to high workfunction difference more depletion in channel and MOSFET off current decreases. In p channel DMG SOI JLT SS is minimum at channel length 40nm. In fig.7 observed that off current of DMG SOI JLT is maximum as compared to with junction transistor due to band to band tunneling. In some channel length SS is maximum of DMG SOI JLT as compared to with junction transistor.

IV. CONCLUSION

In this paper simulate analog performance parameters using 3-D COGENDA TCAD software. Analog performance parameters of DMG SOI JLT compare with DMG SOI Transistor.

- Transconductance g_m of DMG SOI JLT improve by 12% compare to DMG SOI Transistor.
- Transconductance generation factor g_m/I_{DS} of DMG SOI JLT improve by 20% compare to DMG SOI Transistor.
- Output conductance g_d of DMG SOI JLT improve by 69% compare to DMG SOI Transistor.
- Intrinsic gain improved by 21% compare to DMG SOI Transistor.
- Intrinsic static power dissipation of DMG SOI JLT improve by 26% compare to DMG SOI Transistor.

REFERENCES

[1] T. Ohno, Y. Kado, M. Harada and T. Tsuchiya, "Experimental 0.25um gate fully depeleted CMOS/SIMOX process using a new two-step LOCOS isolation technique," *IEEE Trans. Electron Devices*, vol. 42, pp. 1481-1486, Aug. 1995.

[2] W. Long, H. Ou, J. M. Kuo, and K. K. Chin, "Dual material gate (DMG) field effect transistor," *IEEE Trans. Electron Devices*, vol. 46, pp. 865-870, May 1999.

[3] M. Shur, "Split-gate field effect transistor," *Appl. Phys. Lett*., vol. 54, no. 9, pp. 162-164, Jan. 1989.

[4] K. Na and Y. Kim, "Silicon complementary metal-oxide-semiconductor field-effect- transistors with dual work function gate," *Jpn. J. Appl. Physics*., vol. 45, no. 12, pp. 9033-9036, Dec. 2006.

[5] M. Saxena, S. Haldar, and M. Gupta, "Physics-based analytical modelling of potential and electric field distribution in dual material gate (DMG)-MOSFET for improved hot electron effect and carrier transport efficiency," *IEEE Trans. Electron Devices*, vol. 49, no. 11, pp. 1928-1938, Nov. 2002.

[6] C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, "Junction less multigate field-effect transistor," *Appl. Phys. Lett.*, vol. 94, no. 5, pp. 053511-1–053511-2, Feb. 2009.

[7] C.-W. Lee, A. N. Nazarov, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi *et al.*, "Low sub threshold slope in junction less multigate transistor," *Appl. Phys. Lett.*, vol. 96, no. 10, pp. 102106-1–102106-3, Mar. 2010.

[8] C.-W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi *et al.*, "Performance estimation of junction less multigate transistors," *Solid State Electron.*, vol. 54, no. 2, pp. 97–103, Feb. 2010.

[9] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain *et al.*, "Nanowire transistors without junctions," *Nat. Nanotechnology.*, vol. 5, no. 3, pp. 225–229, Mar. 2010.

[10] H. J. Lou, L. N. Zhang, and Y. X. zhu, "A Junction less nanowire transistor with a dual material gate," *IEEE Transaction on Electron Devices*, vol. 59, no. 7, July 2012.

[11] R. Baruah and R. P. Paily, "A dual-material gate junction less transistor with high-K spacer for enhanced analog performance," *IEEE Transaction on Electron Devices*, vol. 61, no. 1, pp. 123-128, Jan. 2014.

[12] V. Kumari, N. Modi, and M. Saxena, "Theoretical investigation of dual material junctionless double gate transistor for analog and digital performance," *IEEE Transaction on Electron Device*, vol. 62, no. 7, pp. 2098-2105, July 2015.

[13] S. Sahay and M. J. Kumar, "Diameter dependence of leakage current in nanowire junctionless field effect transistor," *IEEE Transaction on Electron Devices*, vol. 64, no. 3, pp. 1330-1335, March 2017.

[14] M. Gupta and A. Kranti, "Steep-switching germanium junctionless MOSFET with reduced off-state tunneling," *IEEE Transaction on Electron Devices*, vol. 64, no. 8, pp. 3582-3587, Sep. 2017.

[15] D. Roy and A. Biswas, "Sidewall Spacer layer Engineering for improvement of analog/RF Performance of nano scale double-gate junctionless transistors," *Microsystem Techno*, vol. 23, pp. 2847-2857, 2017.

[16] G. Saini and S. choudhary, "Improving the subthreshold performance of junctionless transistor using spacer engineering," *Microelectronics Journal*, vol. 59, pp. 55-58, 2017.

[17] S. C. Wagaj and Y. V. Chavan, "Nanoscale dual material gate silicon on nothing junctionless MOSFET for improving short channel effect and analog performance," *CCIS*, vol. 628, pp. 27-38, Dec. 2016.
[18] S. C. Wagaj and Y. V. Chavan," "Comparative study of single material gate and Dual material gate silicon-on-insulator junctionless transistor," in *Proc. IEEE Conference Intelligent System and Control*, India, Jan. 5-6, 2017.
[19] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, "A physically based mobility model for numerical simulation of nonplanar devices," *IEEE Transaction Computer-Aided Design*, vol. 7, no. 11, pp. 1164-1170, 1988.
[20] G. C. Patil and S. Qureshi, "Underlap channel metal source/drain SOI MOSFET for thermally efficient low power mixed signal circuits," *Journal of Elsevier Microelectronics*, vol. 43, pp. 321-328, Jan. 2012.

S. C. Wagaj received the B.E. and M.E. degrees in electronics engineering from Shivaji University Kolhapur, Maharashtra, India, in 1999 and 2006 respectively. He is currently pursuing the Ph.D. with modeling and simulation of junction-less transistor for low power and high performance in the JSPM's Rajarshi Shahu College of Engineering Pune, Research Center of Savitribai Phule Pune University, Pune.

He is currently working as an assistant professor at JSPM's Rajarshi Shahu College of Engineering Pune. His research interests include modeling and simulation of novel device structures on SOI Junction-less MOSFETs. He is a life member of Indian Society for Technical Education New Delhi India. He published five papers in international journal and four papers in international conference. He published one Indian patent on shielded channel junctionless transistor in Jan. 2016.

Shailaja Patil is a professor at the Department of Electronics and Telecommunication of RSCOE, affiliated to Savitribai Phule Pune University, Pune. She received the Ph.D. in computer engineering from SVNIT, SURAT. She has total 25 years' research and teaching experience in the field of wireless technologies, internet of things and pervasive computing. She has authored many research articles in international conference and journal, book chapters, patent, and book. She has worked as session chair, reviewer for various national, international conferences. She is a member of professional bodies such as ISTE, IEEE and ACM.