Chip Architecture for Silicon Characterization of Foundry Kit Standard Cells

Siddharth Katare, Ajay Kumar Gautam, Victor John, Rohini V Meti, and Manoj Chitneedi

***Abstract*—Standard cell libraries are an integral part of converting an RTL to a manufacturable physical design. The automatic place and route EDA tools use these characterized standard cell libraries to arrive at an optimal design within given constraints. The correlation between characterized data and the actual behaviour of cells on Silicon is critical for meeting the desired performance of the manufactured chip. In this paper, we present a modular design and measurement method which can be implemented in an ASIC for correlating the characteristics of the standard cell library. This method simplifies the design of the package and the test board and relatively simple test equipment can be used to measure the silicon characteristics. The ASIC presented in this paper was designed in 180nm for characterizing standard cells, which are delivered as part of the foundry design kit.**

***Index Terms*—Standard cell libraries, characterization, silicon correlation, validation.**

I. Introduction

Standard cell library plays a vital role in today's ASIC design. They simplify the process of converting the RTL implementation to the physical design (GDS) which can be used by fabrication houses for manufacturing the ASICs. This conversion process typically involves an automatic placement and routing tool which relies on the characteristics of the standard cells to arrive at an optimal physical design. The correlation between standard cell library model and their silicon performance is critical for the desired functionality of manufactured design. Standard cell libraries are commonly provided by the foundry as part of their Process Design Kit (PDK). These libraries are designed to target particular requirements on timing, power consumption, supply voltage, or other. Each cell of standard library must be carefully designed and characterized for various conditions such as different input slopes, output loads, process corners etc. Once the design is complete, silicon validation is necessary to ensure the matching between designed and manufactured cells.

Standard cell libraries contain various kinds of cells. These cells can be divided in two main categories:

1) **Combinational Cells**: The combination cells are used to implement asynchronous logic. The cells in this family can be further divided into three sub-categories. First sub-category contains inverters and buffers which are used to increase the driving capability of the signal or to reduce the load on the signal driver. Second sub-category contains primitive logic gates such as *NAND*, *AND*, *NOR* etc. and third sub-category contains complex logic gates such as multiplexer, adder, decoder etc.
2) **Sequential Cells**: The sequential cells such as D-flipflop, SR-latch etc. are used to synchronize signals and to store the state of signals.

The automated place and route EDA tool is dependent on the pre-characterized data of standard cell libraries to optimize the circuit design. The availability of a large number of library cells provides larger ASIC design space which improves overall circuit design and area. The standard cell libraries can be enriched by adding new drive strengths [1], through the addition of new functions [2] or even with special transistor topologies [3].

In this paper, we outline the procedure to design an ASIC which is used to validate the characteristics of standard cells. This ASIC was designed in 180nm for characterizing standard cells, which are delivered as part of the foundry design kit. The validation of ASIC covers the functionality check of cells and measurement of timing and power data to fine tune the process models.

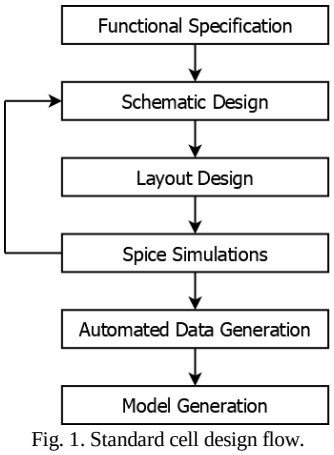

Fig. 1. Standard cell design flow.

II. Standard Cell Design

Fig. shows the standard cell design flow. The design of a standard cell starts by specifying functionality of the cell, delay, power, area, fanout etc. The next step is to create schematic and layout to meet the specifications of the cell. The designed cells are verified by running spice simulation to ensure that the cell meets all the specifications. After the

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The authors are with Sankalp Semiconductor Pvt ltd, Bangalore, India (e-mail: siddharth.katare@sankalpsemi.com, ajay.gautam@sankalpsemi.com, victor.john@sankalpsemi.com, rohini.meti@sankalpsemi.com, manoj.chitneedi@sankalpsemi.com)

design and layout of the cell is finalized, various input and output stimulus conditions such as different input slew rate, different output load, different power supply voltages etc. are applied to the cell to generate their timing and power characteristics. An in-house automation tool was used to generate the data by applying various stimulus conditions. The data generated by these stimulus are captured in different models which are used by EDA tools.

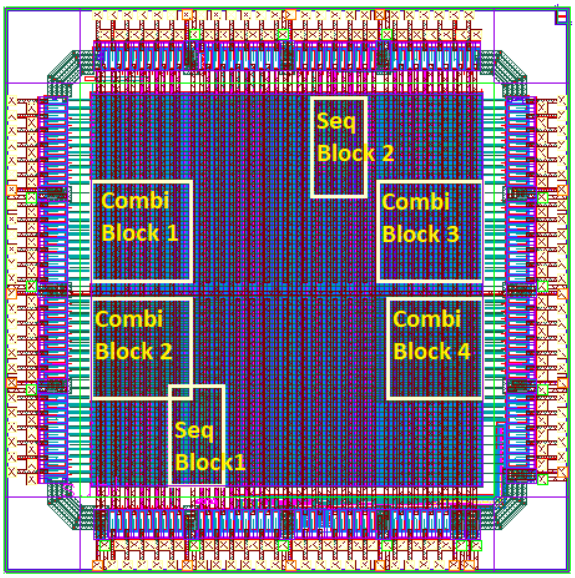

Fig. 2. ASIC layout for standard cell validation.

III. ASIC Design for Standard Cell Verification

An ASIC was designed to correlate the simulation results with silicon results [1], [4]. The ASIC consists of the standard cells along with peripheral circuit required to measure delay and power of an individual standard cell. The combinational cells are divided into four blocks for measurement. The sequential cells are divided in two blocks for measurement. There are additional diagnosis circuitries for measuring the wire delays and loopback mode for verifying the input and output buffers. The ASIC also contains scan chains for checking the stuck-at faults for digital signals.

Fig. 2 shows the layout for the complete ASIC. All the pins are placed at the periphery of the ASIC. The ASIC also includes characterization circuitry for various capacitors provided by the foundry. The rest of the area was populated with decoupling capacitor for better supply noise rejection.

A. Combinational Cells Verification

The delay of a single combination cell lies in the sub nanosecond range. Measuring delay of single cell requires oscilloscopes with very high bandwidth and resolution. In this ASIC, we have used a chain of standard cells to increase the delay as well as average out the impact of random mismatch and noise over multiple cells. This scheme greatly simplifies the package and test board design and relatively simple test equipment can be used for verification of standard cells.

Fig. 3 shows the combinational block verification scheme. The *MUX* and *DEMUX* blocks are used to route the signal from one of *N+1* available path with-in combinational block which are selected by *SEL[k:0]* signal. There are *N* sub-blocks (C_0, C_1, ... C_{N-1}) within each combinational block and one common block (*CMN*). The common block is used to cancel the common delay between input pin and output pins. The inclusion of common block significantly reduces the error in measurement of single cell delay due to cancellation of additional delays between the signal generator and the oscilloscope.

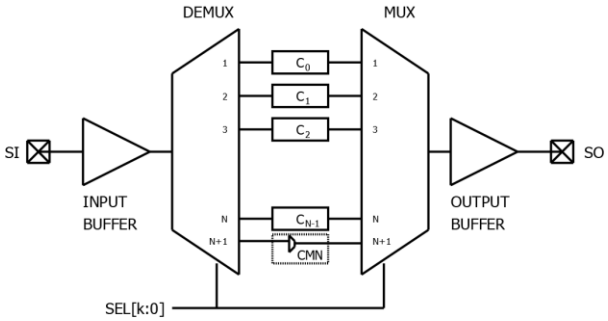

Fig. 3. Combinational block verification scheme.

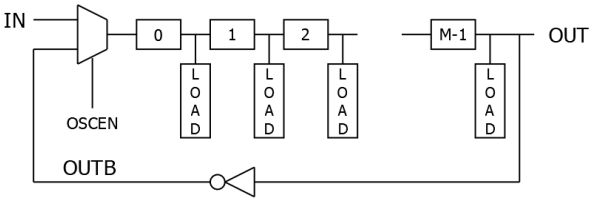

Fig. 4. Combinational sub-block architecture.

Fig. 4 shows the architecture of a sub-block. There are M_i instances of a standard cell are chained together in C_i sub-block. The output of each cell also includes a load block (*LOAD*) which is used to measure delay for different output conditions. The sub-block also contains a multiplexer to configure the sub-block in the ring oscillator mode which is used for diagnosis. The delay (td_i) from *SI* to *SO* for i^{th} sub-block can be express by following equation

$$td_i = td_N + M_i \times td_{Ci} \quad (1)$$

where, td_{Ci} is delay of single standard cell in the i^{th} sub-block. The td_N is delay from *SI* to *SO* for the *CMN* path.

We can rearrange (1) to get delay of a single standard cell as:

$$td_{Ci} = \frac{td_i - td_N}{M_i} \quad (2)$$

A similar expression can be derived for the power measurement. Following equation can be used to calculate the power consumed by a single standard cell:

$$P_{Ci} = \frac{P_i - P_N}{M_i} \quad (3)$$

where, P_{Ci} is power of single standard cell in the i^{th} sub-block. The P_N is power for the *CMN* path and P_i is power of the i^{th} path.

B. Sequential Cells Verification

Similar to combinational blocks, measuring the clock-to-Q

delay of individual sequential cell requires oscilloscopes with very high bandwidth and resolution. One possible method to measure such delay is configuring the sequential cells in the ring oscillator mode [5]. In this method, the ring oscillator operating frequency depends directly on the different delay arcs related to the cell under test.

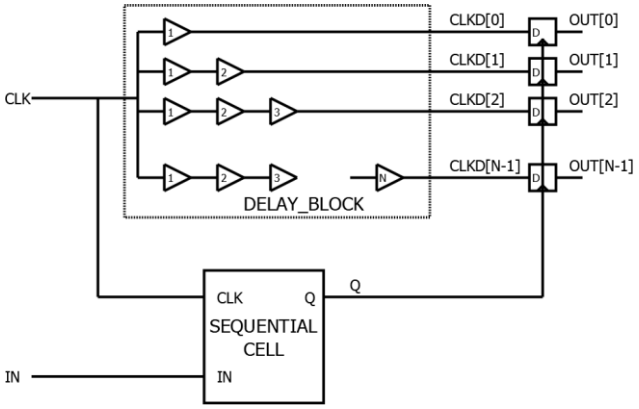

Fig. 5. Sequential block verification scheme.

The other method to measure the clock-to-Q delay is to use time-to-digital converter architecture [6]. This architecture is implemented in the ASIC as shown in Fig. 5. The *DELAY_BLOCK* is used to generate multiple delayed versions of the *CLK* signal which is used as the trigger for the sequential cell under test. The outputs of the *DELAY_BLOCK* are *N* clocks *CLKD[N-1:0]*, each consecutive signal is apart by two inverter delay. The *DELAY_BLOCK* is characterized using the same scheme as combinational block characterization.

The *N* clock signal are connected to *D* terminal of positive edge triggered D-flipflops. The *CLK* terminal of the flipflops is connected to *Q* signal of the sequential cell under test. The output of these D-flipflops *OUT[N-1:0]* are used to determine the clock-to-Q delay of the sequential cell under test. Once the data is captured by D-flipflops, there will be *k* out of *N*, *OUT* signal will be high i.e. *OUT[k-1:0]* will be high and *OUT[N-1:k]* will be low. The clock-to-Q (t_{ckq}) delay is then calculated in terms of single inverter delay (td_{inv}) as:

$$t_{ckq} = 2 \times k \times td_{inv} \quad (4)$$

The value of inverter delay defines the resolution of the delay measurement while *N* decides the range of the delay measurement. The value of *N* is chosen such that it can measure up to 25% increase in clock-to-Q delay from ∞ setup and hold time to calculate the minimum setup and hold time for sequential cell.

C. Diagnostic Circuits

The design ASIC also contains several diagnostic circuits which are helpful in narrowing down the root cause of any erratic behaviour observed on the silicon.

1) **Scan Chains**: There are several digital circuits on ASIC which are used to select the combinational and sequential cells for test. It is important to ensure that the select signals are as expected during silicon characterization of standard cells. The scan chains are used to monitor these signals on scope to ensure that the right cells are getting selected by these select signals.
2) **Wire Delay Measurement**: The resistance and capacitance of connecting metal wires play important role in delay of standard cells. The wire delay measurement circuit helps in eliminating any mismatch between extracted wire parasitic and silicon parasitic. The wire delay measurement contains circuit contains traces of different metals connected between input and output pads. The delay between input and output can be measured to correlate the wire delay between simulation and silicon in case of any mismatch.
3) **Combinational Block Self Test**: The combinational blocks have a self test mode in which sub-blocks can be configured as ring oscillators. Each of sub-blocks can be configured in ring oscillator mode using *OSCEN* signal. Ring oscillator mode helps is correlating the delay of cells with the oscillation frequency. This feature is used as debug mode during silicon validation stage for eliminating dependency on external circuits which drives the delay chain.

IV. Silicon Validation

The ASIC die was manufactured in 180nm CMOS process. The die was packaged in 208 pins PGA package. The bench validation contains two PCBs, which help in the reuse of the signal board for multiple variants of ASIC. Riser PCB is used to mount the packaged part and to convert package PGA pitch to standard connector pitch for easy access to all the pins of the ASIC. The signal board contains connectors for applying time varying signals and control signals to configure the device and select the cell for test. The control signals are generated by the microcontroller board for automated test and measurement. A signal generator is used to apply the clock and the data signals and an oscilloscope is used to capture different signals for delay measurement. A thermostream is used for measurement across various temperatures. The complete setup is shown in Fig. 6.

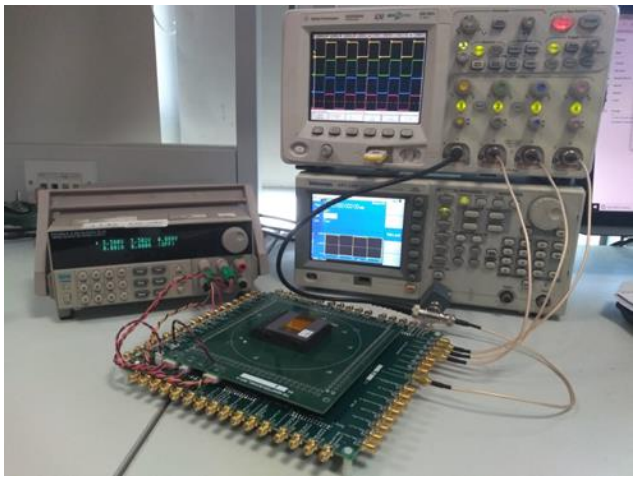

Fig. 6.Test setup for silicon measurement.

Fig. 7 shows the scope shot for combinational block measurement. When the *OSCEN* signal is **0**, the delay

between input and output pin is measured by applying a step on the input pin. The delay of common path is subtracted from measured delay and divided by the number of cells in the sub-block under test to compute the delay of a single cell. When the *OSCEN* signal is **1**, the combinational block is configured in ring oscillator mode. The output pin in this case is used to measure the frequency of the oscillation. Fig. 8 shows the comparison between the simulated delay and the measured delay for various combinational cells for two different dies.

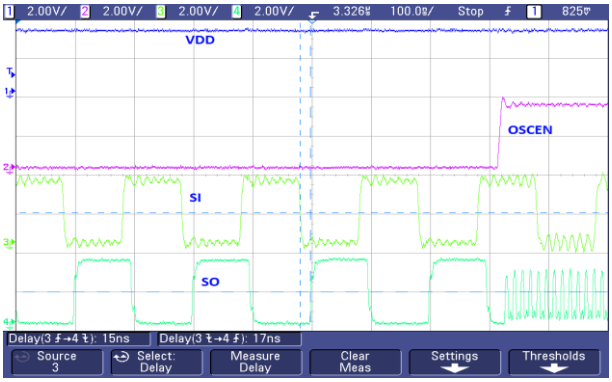

Fig. 7. Delay measurement for a combinational cell.

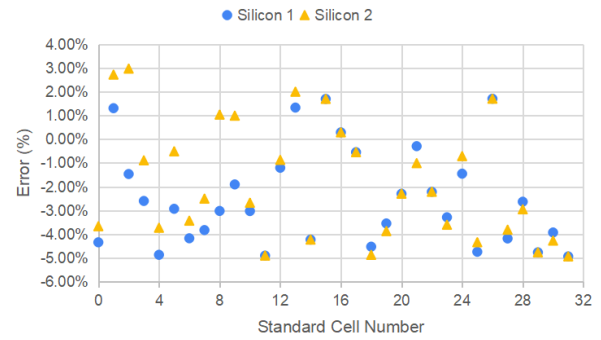

Fig. 8. Simulation vs silicon results for combinational cells.

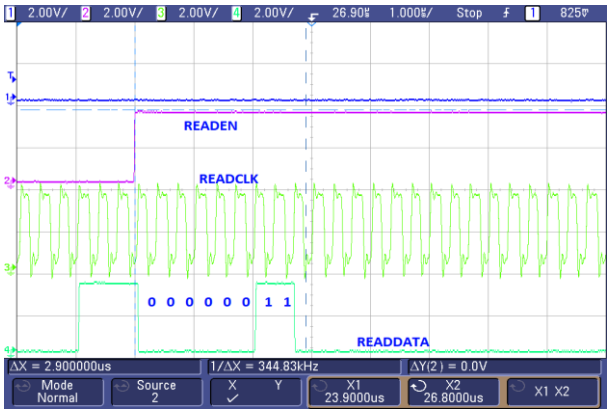

Fig. 9. Clock-to-Q measurement for a sequential cell.

The sequential cell clock-to-Q delay is captured internally using the *DELAY_BLOCK* and D-flipflops. The value of these D-flipflops are read out serially on the output pin to determine the clock-to-Q delay for a sequential cell under test. The Fig. shows a scope shot for one such measurement. The *READCLK* is used to clock the serial readout path while *READDATA* provides values of *OUT[N-1:0]* signal. Fig. shows a case for *N*=**8**. The *OUT[7:0]* is **8'b00000011** which translates to 4 inverter delay using (4).

V. Conclusion

In this paper, we have presented architectures for designing an ASIC which can be used to characterize the standard cells provided by the foundry as part of their process development kit. The individual standard cells were characterized using spice simulations. The ASIC incorporated a circuit scheme which simplified the design of the package and the test board and relatively simple test equipment could be used to measure the silicon characteristics. The results are presented here for comparison between simulation and measured delays. The paper also outlines some of the diagnostic features which were included in the ASIC for narrowing down the root cause of any erratic behaviour observed on the silicon.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Siddharth and Ajay worked on the design and simulation for standard cells. Rohini worked on layout of standard cells. Victor and Manoj worked on silicon validation for the standard cells. Siddharth wrote the paper for this standard cell verification methodology.

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Siddharth Katare received his master of technology degree in electical engineering from Indian Institute of Technology Madras, Chennai in 2007. He has worked in various semiconductor companies such as cypress semiconductor, intel technology, samsung electronics etc. His current role in Sankalp Semiconductor include design and development of analog circuits. His research interests include high speed interface design, SoC integration, power management and high precision analog circuits.

Ajay Kumar Gautam receiver his ME in VLSI technology from University of Roorkee (Now IIT Roorkee), Roorkee, India in 1997. He has worked in various division of STMicroelectronics. He has worked on programmable logics including GOSPL and PiCoGA, memory, logic library (including programmable) and phy characterization and packaging. Presently, he is handling technology foundation group of Sankalp Semiconductor. His interests include programmability in logic or circuits.

Victor John received his BSc in computer engineering from Annamalai University, India. He has over 30 years' work experience in various companies and some of them are BEL - Bharat Electronics Limited, MAP-Micro Avionics and Positioning system, MIL-Microcon International Limited, Purple Vision, TES-THALES Electronics Solutions.

Currently he works with Sankalp semiconductor as system architecture providing solutions from specification to production across various domains like aeronautical, industrial, automotive, telematics, IoT and SoC validation, automation environment. He worked on initiatives in India such as AVLS GPS tracking solution, Proprietary Bluetooth Audio layer IO prior. He was a part of the team that developed GPS+GLONASS Navigation system, proprietary hardware Interface system(GPS+DGPS) to carry out live Ship Sea trials for HSL - Hindustan ShipYard Limited.

Rohini V Meti received her master of technology degree in digital electronic from BVB College of Engineering and Technology in 2016. She has been working in Sankalp Semiconductor as a layout design engineer. Her research interests include design of standard cells, custom layouts and physical verification.

Manoj Chitneedi received his bachelor of technology degree in electronics and communication engineering from Jawaharlal Nehru Technological University, Hyderabad in 2018. He has been working in Sankalp Semiconductor as a hardware engineer and executed Post Silicon Validation activities of Foundry kit Standard cells, CDR chip with MIPI D-PHY, C-PHY interface, PMIC IC's comprising of LDO, Boost and Buck-Boost regulators. His research interests include high speed LVDS blocks characterization and Bench validation of Power IC's.