Production Rate Based Dynamic Dispatching Rule Selection in a Wafer FAB

Yong H. Chung, Won K. Ham, and Sang C. Park

***Abstract*—This paper proposes a state-dependent dispatching rule to achieve on-time delivery as well as minimum of mean cycle time in a wafer FAB. Dispatching rule should be selected dynamically according to current system state and operation objective, since condition in a wafer fab is dynamically changed. In this paper, we use 'pegging' to identify a current state of a wafer FAB. Pegging is defined as the process of assigning wafer lots to orders, and it is very essential to meet customers' demands in terms of quality, quantity, and due dates in a wafer FAB. As a result, pegging decides target move for each step, it is necessary to select WIP lot to be processed next. The proposed state-dependent dispatching rule consists of two stages. At the first stage, WIP lots are classified into two groups which has priority, and classical dispatching rule is applied to select a WIP lot at the second stage. The target move and actual move are computed by the combination of pegging and simulation. We developed a simulation model by using MIMAC6, and conducted simulation with SEEPLAN®.**

***Index Terms*—State-dependent dispatching rule, simulation, wafer FAB, pegging.**

I. Introduction

To be successful in the globalized competition, chip manufacturers have been developed technology such as larger wafer sizes and smaller chips. However, the production in a wafer fabrication (FAB) is considered as one of the most complex manufacturing processes because of reentrant processing flow, batch processing, sequence dependent setups, unpredictable tool failure. Thus, if not managed properly, the highly complex attribute of semiconductor manufacturing can result in high levels of work-in-process (WIP), long cycle times, and poor due-date performance [1].

Dispatching is defined as determining a WIP lot to be processed next, whenever a tool becomes available state, as shown in Fig. 1. It is one of the major techniques to achieve to smooth manufacturing process, lower inventory level and meet due date, so it is used as tool for shop floor control because of the ease of implementation, quick in reacting to the changes encountered on the shop floor, low computation requirement, and flexibility to incorporate domain knowledge and expertise. [2] The classical dispatching rules like First in First out (FIFO), Operation due date (ODD), Earliest due date (EDD), Critical Ratio (CR) have been adopted in wafer FABs.

Although there are various classical dispatching rules, most of the classical dispatching rules do not pay much attention on various situations for a wafer FAB. Furthermore, there is no classical dispatching rule that always achieves on-time delivery and minimum of mean cycle time for all situations. To overcome the limitation, quite a few researchers have tried to develop the dispatching rule that determines WIP lot by considering the state of a wafer FAB. [3] In 2001, Bo-Wei Hsieh *et al.* developed an ordinal optimization-based simulation tool designed to dynamically select scheduling rules for semiconductor wafer fabrication when machine failures and temporary holding of WIPs from processing due to engineering causes occurs. The dispatching rule may be weekly selected based on fab states over a four-week horizon. [4] In 2002, Tyan, J. C. *et al.* developed state-dependent dispatching rule based on the theory of constraints. Three state variables (machine utilization, machine queue length, and contention factor) and three dispatch rules (two boundary, shortest time to next visit, and fastest time for next visit) are considered to construct the dispatch rule. [5] In 2004, J. C. Chen *et al.* proposed a dynamic state-dependent dispatching rule that uses different dispatching rules according to the state of a production system. The proposed dispatching rule first classifies workstations into dynamic bottlenecks and non-dynamic bottlenecks. Dynamic bottleneck workstations apply a revised two-boundary dispatching rule when their queue length exceeds the average obtained from simulation using constant lot-release policy and first-in, first-out dispatching rule. Otherwise, the shortest expected processing time until next visit dispatching rule is used. [6] To conclude from the previous work on the topic of state-dependent dispatching rule, as conditions dynamically change in a wafer FAB, a dispatching rule that adapts to these conditions is more likely to perform better than a static rule.

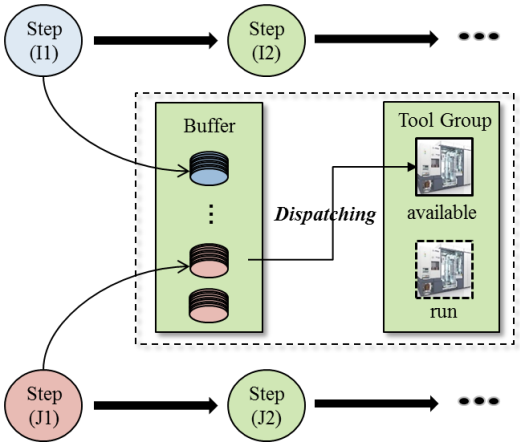

Fig. 1. Role of dispatching.

In this paper, we propose state-dependent dispatching rule that selects dispatching rule by considering states dynamically change in a wafer FAB to achieve on-time delivery and to

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minimize mean cycle time. In developing the proposed dispatching rule, the major challenge is to recognize the system state in a wafer FAB. The proposed dispatching rule employs the combination of pegging and simulation to recognize the system state. While time of simulation goes forward, the time of pegging goes backward. As shown in Fig. 2, if simulation cycle is a 1 day, pegging also will be performed at start time per 1 day. As a result of the simulation, we can have the in-actual record and WIP for each step. Pegging is defined as the process of assigning wafer lots to orders, and it is very essential to meet customers' demands in terms of quality, quantity, and due dates in a wafer FAB. It determines in-target for each step, and calculates the latest possible start time (LPST) for each lot, as shown in Fig. 3. Usually, we use pegging to acquire the release plan to meet the in-target considering current WIP and machine status.

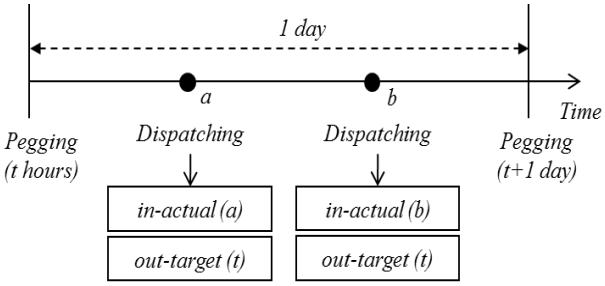


Fig. 2. Combination of pegging and simulation.

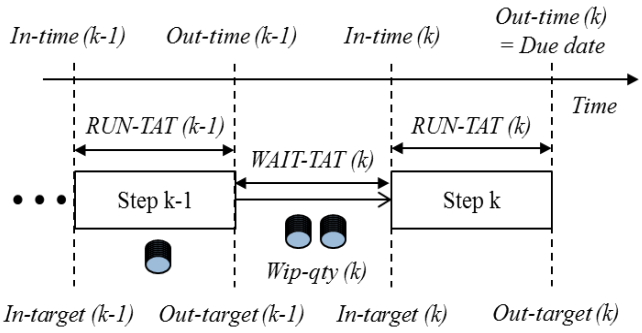


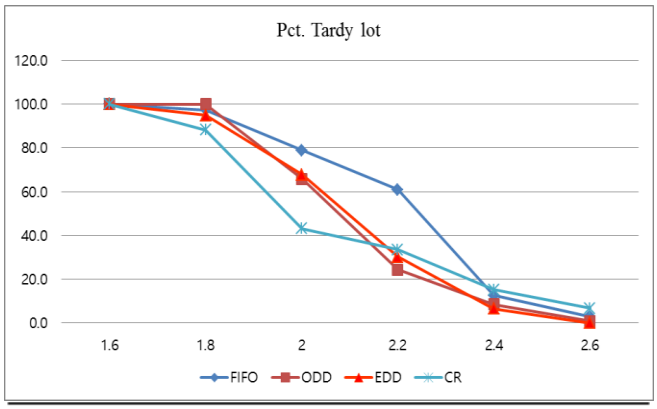
Fig. 3. In/Out target for each step.

The objective of this paper is to develop state-dependent dispatching rule to achieve on-time delivery and to minimize mean cycle time in a wafer FAB. The key idea of this paper is to applying the combination of pegging and simulation to determine the dispatching rule by considering states dynamically change of a wafer FAB, whenever a tool determines a lot to be processed next. For the execution of the pegging and simulation, we used a commercial software SEEPLAN® developed by the VMS solutions [7] The remainder of this paper is organized as follows. Section II addresses the approach of this paper for the state-dependent dispatching rule, and Section III describes the experimental design and analyzes experimental results. Finally, summary are given in Section IV.

II. Approach to Develop State-Dependent Dispatching Rule

In this Section II, we will compare the FIFO, ODD, EDD, and CR. The simulation length of MIMAC6 was carried out for 8 months, The first 6 months were considered as warm-up periods, and not taken into account for statistic. We simulated the fab, under 93% FAB capacity loading and with flow factor ranging from 1.6 to 2.6 in steps of 0.2. Flow factor is defined as the target cycle times divided by the raw processing time. It is necessary to build various state of a wafer FAB. With regard to on-time delivery and mean cycle time, simulation results show that CR outperforms FIFO, EDD, and ODD with tight target due date (1.6-2.0). It does not, however, provide on-time delivery and mean cycle time as good as EDD. Since CR and EDD show better performance measure with different state, the performance of a modified combination of these rules is of interest. The paper attempts to combine different dispatching rules with good performance in terms of various performance measures. The proposed state-dependent dispatching rule employs CR and EDD to achieve on-time delivery and to minimize mean cycle time.

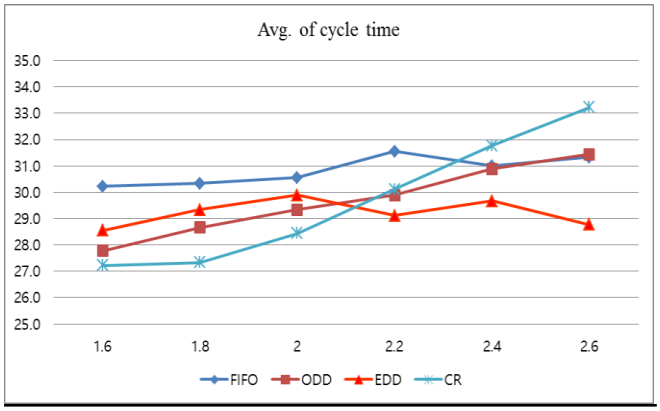
$$\text{Production Rate}_k = \text{in-actual}_k / \text{in-target}_k \quad (1)$$



Pct. Tardy lots (%)

	1.6	1.8	2	2.2	2.4	2.6	Average
FIFO	100.0	97.4	79.0	60.9	12.5	3.0	58.8
ODD	100.0	100.0	65.8	24.3	8.4	0.7	49.9
EDD	100.0	95.0	67.8	30.2	6.5	0.0	49.9
CR	100.0	88.2	43.2	33.4	15.2	6.7	**47.8**

Fig. 4. On-time delivery comparison of with 4 dispatching rules.



Avg. Cycle time (days)

	1.6	1.8	2	2.2	2.4	2.6	Average
FIFO	30.2	30.3	30.6	31.6	31.0	31.3	30.8
ODD	27.8	28.7	29.3	29.9	30.9	31.4	29.7
EDD	28.6	29.3	29.9	29.1	29.7	28.8	**29.2**
CR	27.22	27.33	28.44	30.11	31.78	33.22	29.7

Fig. 5. Mean cycle time comparison of with 4 dispatching rules.

The focus of this paper is to recognize the state dynamically changed in a wafer FAB. We can acquire in-target and in-actual by combination of pegging and simulation, as shown in Fig. 2. The production rate of each step can be calculated by in-target and in-actual. Equation (1) defines the production rate of step k, where in-actual and in-target is decided by simulation and pegging, respectively. The production rate is very essential to achieve on-time delivery for a wafer FAB. The proposed dispatching rule can be classified into two stages. It first take into account the production rate of each step, and CR or EDD dispatching rule select a WIP lot to be processed next at second stage. Fig. 6 shows the structure of the proposed dispatching rule. If any lot that production rate of corresponding step is under 1.0 exist in the queue, then one of these lots is selected using CR. If no such lots exist, then one of these lots is selected using EDD. If there are lots having highest priority, then the proposed dispatching rule determine a lot using FIFO rule.

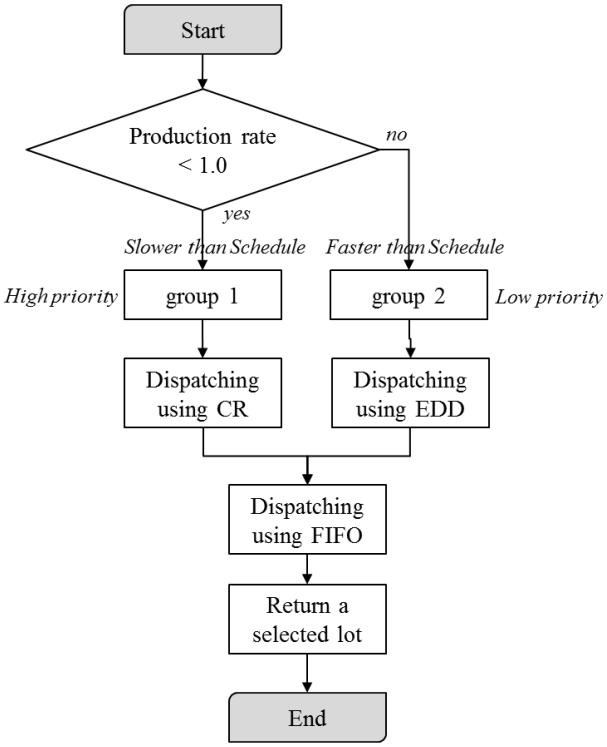


Fig. 6. Procedure of the proposed dispatching rule.

III. Simulation Result

Simulation results demonstrate that a dispatching rule significantly influences all performance measures. This work investigates on-time delivery and mean cycle time with various dispatching rules under the small wafer fab dataset MIMAC6 from Measurement and Improvement of Manufacturing Capacities (MIMAC). MIMAC6 is a typical complex wafer fab model. As shown in Fig. 7, the FAB consists of 104 tool groups, and produce 9 products having different process. The product having longest steps has 355 steps, and the shortest one has 247 steps. A lot consists of 24 wafers, and 2777 lots are released per year under fab loading of 100%.

The simulation experiments are carried out with SEEPLAN® developed by the VMS solutions. Fig. 8 shows how the SEEPLAN® engine generates loading schedule for each tool in the FAB. It requires three master data: bill of process (BOP) model, resource model, and dispatching rule. The current WIP is initialized at the beginning of simulation. Considering the current WIP, release plan is used as an input. The simulation results can be analyzed to see the performance measures including resource utilization, throughput, and WIP fluctuations.

Data	Value
Tool groups	104
Tools	228
Wafers in a lot	24
Wafers released per year	2777
Process steps	9
Steps	2241
Average number of steps of products	249
Longest steps among process steps	212
Average processing time of steps (sec)	3014

Fig. 7. Fab model.

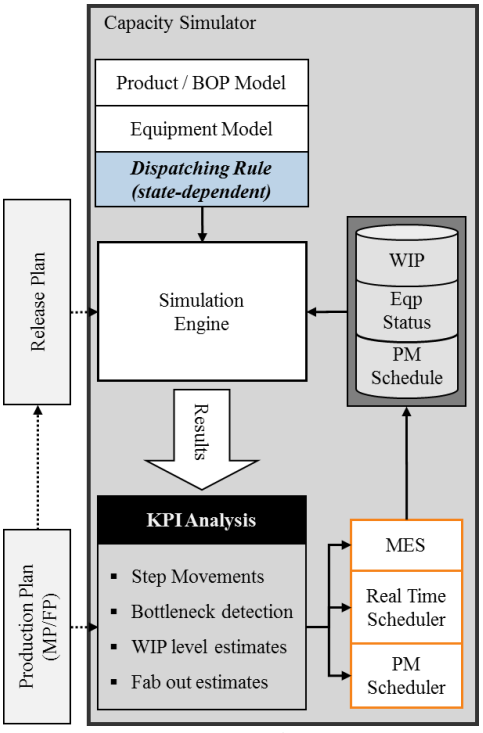


Fig. 8. Architecture of SEEPLAN.

BOP model is a network model which combines BOM (bill of material) and process routing. It consists of parts, processes, and transitions. BOP model contains step sequence, loadable resource list, and run time and wait time for each step, and transfer time. A resource is characterized by handling unit, process type, and defect treatment policy. Resource group (tool group) indicates standard step to be processed, jig capacity, setup crew capacity, and list of unit resources (tools). Each resource has dispatching rule and processing time. Dispatching rules are used to determine the priority for meeting customer orders. As shown in Fig. 9, MIMAC6 data set is imported into FAB model of SEEPLAN®.

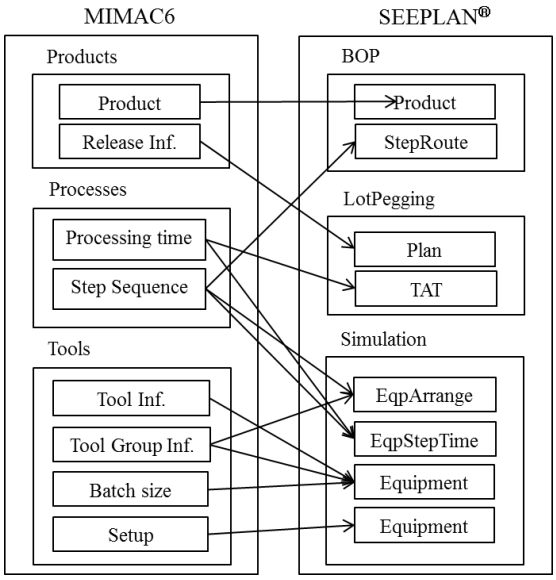
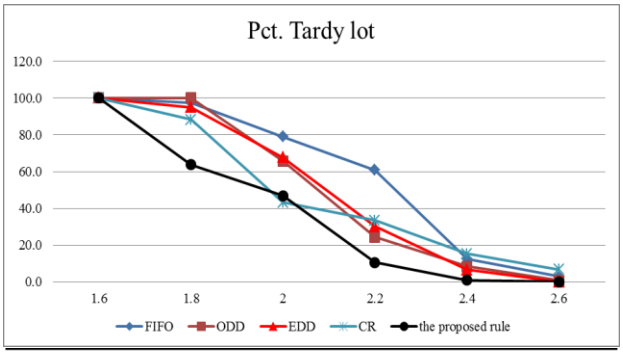


Fig. 9. From MIMAC6 to SEEPLAN.



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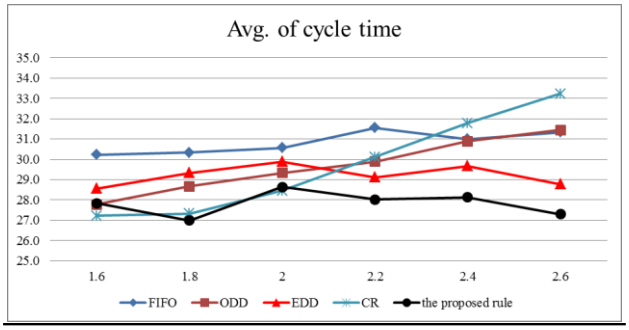
CR	100.0	88.2	43.2	33.4	15.2	6.7	**47.8**
The proposed rule	100.0	63.6	46.8	10.6	0.9	0.0	**37.0**



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CR	27.22	27.33	28.44	30.11	31.78	33.22	29.7
The proposed rule	27.8	27.0	28.6	28.0	28.1	27.3	27.8

Fig. 10. Performance measures comparison with 4 classical dispatching rule and the proposed dispatching rule.

We take account into mean cycle time, tardy lot percentage as major performance measures. Fig. 10 shows this 2 performance results. The proposed dispatching rule's average cycle time curve has a similar trend like CR and EDD respectively on tight due date flow factor, loos due date flow factor. It has minimum value with regard to average tardy lot percentage and average cycle time among 5 dispatching rules. The maximum average cycle time exits in flow factor 2.0, and the minimum average cycle time exits in flow factor 1.8. The most important thing is no matter with flow factor, the proposed dispatching rule outperforms FIFO, ODD, and EDD.

IV. Summary

The highly complex attribute of semiconductor manufacturing can result in high levels of work-in-process (WIP), long cycle times, and poor due-date performance. The role of dispatching is to determine a WIP lot to be processed next, when a tool becomes available. It is one of the major techniques to achieve to smooth manufacturing process, lower inventory level and meet due date. It is used as tool for shop floor control because of the ease of implementation, quick in reacting to the changes encountered on the shop floor, low computation requirement, and flexibility to incorporate domain knowledge and expertise. There have been various classical dispatching rules like FIFO, ODD, EDD, CR.

As states dynamically change in a wafer FAB, a dispatching rule that adapts to these conditions is likely to outperform a static dispatching rule. There have been various dispatching rules consider state of a wafer FAB. The focus of these works is to identify state dynamically change in a wafer FAB. In this paper, we use the combination of pegging and simulation. The production rate is very essential to achieve on-time delivery for a wafer FAB. It is necessary to calculate the production rate of each step to identify FAB's state. The proposed dispatching rule consists of two stages. It first take into account the production rate of each step, and CR or EDD dispatching rule select a WIP lot to be processed next at second stage. For the experimentation of the proposed state-dependent dispatching rule, we used a commercial software SEEPLAN® developed by the VMS solutions.

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